L24 ANSWER 31 OF 60 CA COPYRIGHT 2002 ACS
AN 131:66520 CA
TI Semiconductor device and fabrication thereof
IN Takubi, Atsushi
PA Nippon Steel Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11177058	A2	19990702	JP 1997-356228	19971209

AB ~~The invention~~ relates to a semiconductor device, i.e., a DRAM LSI, wherein the **SiO2-BPSG interlayer** dielec. film is **planarized** by chem.-mech. **polishing**, followed by **etch-back**.

L1: Entry 3 of 8 File: DWPI Jul 2, 1999

DERWENT-ACC-NO: 1999-435970
DERWENT-WEEK: 199937

TITLE: Semiconductor device formation method e.g. for DRAM - involves etching second insulating film which is polished by CMP method and then further polishing etched film, so that first insulating film is exposed

PRIORITY-DATA: 1997JP-0356228 (December 9, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 11177058 A	July 2, 1999		014	H01L027/108

INT-CL (IPC): H01 L 21/8242; H01 L 27/108

ABSTRACTED-PUB-NO: JP11177058A
BASIC-ABSTRACT:

NOVELTY - Two insulating films (12,13) are formed sequentially on memory cell formed on element isolation structure (22). The insulating film (13) which is thicker than insulating film (12), is polished by CMP method so that its surface becomes flat. Then etching of the insulating film (13) is performed followed by further polishing, so as to expose part of insulating film (12).

DETAILED DESCRIPTION - The element isolation structure is formed on element isolation area of a semiconductor substrate (1).

USE - For DRAM manufacture.

ADVANTAGE - Ensures sufficient flatness of memory cell, thereby enabling manufacture of high density memory cell.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view indicating manufacture of DRAM. (1) Semiconductor substrate; (12,13) Insulating films; (22) Element isolation structure.

L27 ANSWER 10 OF 33 JAPIO COPYRIGHT 2002 JPO
AN 1999-177058 JAPIO
TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURE
IN TAKUBI ATSUSHI

PA NIPPON STEEL CORP
PI JP 11177058 A 19990702 Heisei
AI JP1997-356228 (JP09356228 Heisei) 19971209
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99
AB PROBLEM TO BE SOLVED: To further increase the degree of integration of a semiconductor device, such as the DRAM, etc., having large steps between memory cell sections and their peripheral circuit sections by sufficiently flattening the steps by a simple method.
SOLUTION: In a method for manufacturing a semiconductor device, the surface portion of an **interlayer** insulating film 13 which covers a field shield 22 or a gate electrode structure 23 through an **interlayer** insulating film 12 composed of a silicon **oxide** film and is composed of a **BPSG**(boro-phospho- **silicate** glass) film is removed by about 100-200 nm in thickness by the chemical mechanical **polishing**(CMP) method. When the surface portion of the film 13 is **polished**, the surface is flattened to a some degree. Then the film 13 is **etched back** by using the highest part of the insulating film 12 as a stopper. When the film 13 is **etched back**, the film 13 is sufficiently flattened.

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平11－177058

(43)公開日　平成11年(1999)７月２日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　27/108		Ｈ０１Ｌ　27/10	６８１Ｆ
21/8242			６２１Ｚ

審査請求　未請求　請求項の数14　ＦＤ　（全 14 頁）

(21)出願番号　特願平9－356228

(22)出願日　平成９年(1997)12月９日

(71)出願人　000006655
新日本製鐵株式会社
東京都千代田区大手町２丁目６番３号

(72)発明者　田首　篤
東京都千代田区大手町２－６－３　新日本製鐵株式会社内

(74)代理人　弁理士　國分　孝悦

102b ---- (12-14, 17-18, 20-21)

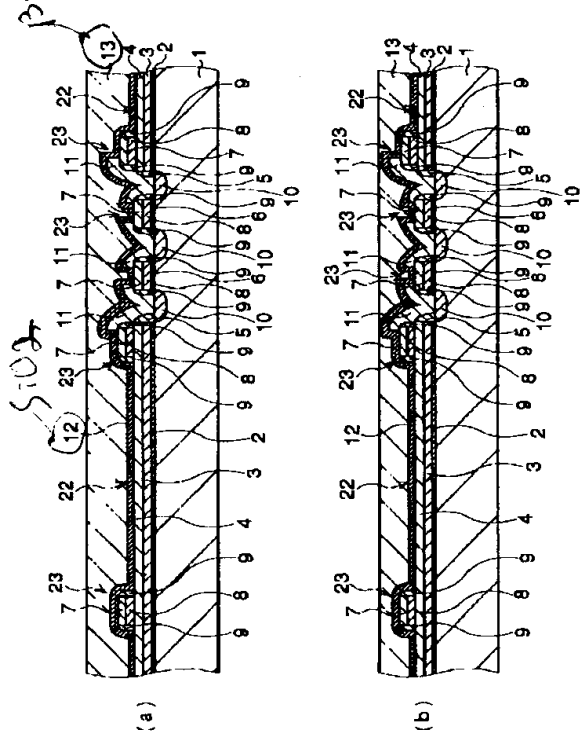
103 ---- (5-16, 22-26, 28-30)

(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】

【課題】　例えばＤＲＡＭのようにメモリセル部と周辺回路部との間に大きさ段差を有する半導体装置において、簡便な手法により十分な平坦化を得ることができ、更なる高集積化の実現を可能とする。

【解決手段】　先ず、フィールドシールド２２やゲート電極構造２３をシリコン酸化膜からなる層間絶縁膜１２を介して覆うＢＰＳＧ膜からなる層間絶縁膜１３を化学機械研磨法（ＣＭＰ法）により表層部位、例えば膜厚１００～２００ｎｍ程度だけ研磨除去する。このとき、層間絶縁膜１３はその表面がある程度平坦化された状態にある。続いて、最も高い位置に存する１２の部位をストッパーとして、層間絶縁膜１３をエッチバック処理する。このとき、層間絶縁膜１３は十分に平坦化された状態にある。



1

【特許請求の範囲】

【請求項1】　半導体基板上の素子分離領域に素子分離構造を形成する第1の工程と、

上記素子分離構造により囲まれて画定された素子形成領域を含む上記半導体基板上に半導体素子を形成する第2の工程と、

前記半導体素子上を含む前記半導体基板の全面を覆うように第1の絶縁膜を形成する第3の工程と、

前記半導体素子を埋め込むように、前記第1の絶縁膜上に当該第1の絶縁膜に比して厚い第2の絶縁膜を形成する第4の工程と、

前記第1の絶縁膜上に前記第2の絶縁膜が残り且つ前記第2の絶縁膜の表面が平坦化されるように前記第2の絶縁膜を研磨する第5の工程と、

前記第1の絶縁膜の一部が最初に露出するまで前記第2の絶縁膜の全面をエッチバックし、前記第2の絶縁膜の表面を平坦化する第6の工程とを有することを特徴とする半導体装置の製造方法。

【請求項2】　前記半導体素子が、メモリセルを構成する第1の素子と、前記メモリセルの周辺回路部を構成する第2の素子とからなることを特徴とする請求項1に記載の半導体装置の製造方法。

【請求項3】　前記第1の絶縁膜がシリコン酸化膜又はシリコン窒化膜からなることを特徴とする請求項1又は2に記載の半導体装置の製造方法。

【請求項4】　前記第6の工程の後に、前記第2の絶縁膜上に第3の絶縁膜を形成する第7の工程を更に有することを特徴とする請求項1～3のいずれか1項に記載の半導体装置の製造方法。

【請求項5】　半導体基板上の素子分離領域に素子分離構造を形成する第1の工程と、

上記素子分離構造により囲まれて画定された素子形成領域を含む上記半導体基板上に半導体素子を形成する第2の工程と、

前記半導体素子を埋め込むように層間絶縁膜を形成する第3の工程と、

前記半導体素子上に前記層間絶縁膜が残り且つ前記層間絶縁膜の表面が平坦化されるように前記層間絶縁膜を研磨する第4の工程と、

前記層間絶縁膜内に埋め込まれた前記半導体素子の構成要素となる各導電膜のうち、最上層の前記導電膜上に形成されたキャップ絶縁膜の一部が最初に露出するまで前記層間絶縁膜の全面をエッチバックし、前記層間絶縁膜の表面を平坦化する第5の工程とを有することを特徴とする半導体装置の製造方法。

【請求項6】　前記半導体素子が、メモリセルを構成する第1の素子と、前記メモリセルの周辺回路部を構成する第2の素子とからなることを特徴とする請求項5に記載の半導体装置の製造方法。

【請求項7】　前記最上層の前記導電膜上に形成された

2

前記キャップ絶縁膜がシリコン酸化膜又はシリコン窒化膜からなることを特徴とする請求項5又は6に記載の半導体装置の製造方法。

【請求項8】　前記第5の工程の後に、前記層間絶縁膜上に上層絶縁膜を形成する第6の工程を更に有することを特徴とする請求項5～7のいずれか1項に記載の半導体装置の製造方法。

【請求項9】　素子分離構造により囲まれて画定された素子形成領域を含む半導体基板上に半導体素子が形成されてなる半導体装置において、

前記半導体素子上を含む前記半導体基板の全面を覆うように形成された第1の絶縁膜と、

前記半導体素子を埋め込むように、前記第1の絶縁膜上に当該第1の絶縁膜に比して厚く形成された第2の絶縁膜とを備え、

前記第2の絶縁膜の表面には少なくとも前記第1の絶縁膜の最上部に位置する一部位が露出しているとともに、前記第2の絶縁膜の前記表面が平坦化されていることを特徴とする半導体装置。

【請求項10】　前記半導体素子が、メモリセルを構成する第1の素子と、前記メモリセルの周辺回路部を構成する第2の素子とからなることを特徴とする請求項9に記載の半導体装置。

【請求項11】　前記第1の絶縁膜がシリコン酸化膜又はシリコン窒化膜からなることを特徴とする請求項9又は10に記載の半導体装置。

【請求項12】　素子分離構造により囲まれて画定された素子形成領域を含む半導体基板上に半導体素子が形成されてなる半導体装置において、

前記半導体素子を埋め込むように形成された層間絶縁膜を備え、

前記層間絶縁膜の表面には、前記半導体素子の構成要素となる各導電膜のうち、最上層の前記導電膜上に形成されたキャップ絶縁膜の一部位が露出しているとともに、前記層間絶縁膜の前記表面が平坦化されていることを特徴とする半導体装置。

【請求項13】　前記半導体素子が、メモリセルを構成する第1の素子と、前記メモリセルの周辺回路部を構成する第2の素子とからなることを特徴とする請求項12に記載の半導体装置。

【請求項14】　前記最上層の前記導電膜上に形成された前記キャップ絶縁膜がシリコン酸化膜又はシリコン窒化膜からなることを特徴とする請求項12又は13に記載の半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、半導体装置及びその製造方法に関し、例えばDRAM等の如くメモリセルとその周辺回路部に著しい段差が存する半導体装置に適用して特に好適なものである。

3

【0002】

【従来の技術】近年、半導体装置の高集積化に伴い、水平方向の微細化は進行しているものの、それに比して垂直方向の薄膜化は、層間絶縁膜の絶縁性の確保や配線の抵抗低減が課題となってさほど進んでいない現状にある。このため、DRAM等の半導体記憶装置を例にとれば、ゲート配線や絶縁膜が高密度に積層されたメモリセル部分と、当該メモリセル部分を制御する周辺回路部分との間に著しい段差が生じ、上層配線やコンタクト孔のフォトリソグラフィー工程におけるパターニング時に寸法のバラツキや解像不良が発生する。この段差を解消するため、メモリセル部分上及び周辺回路部分上を含む全面にBPSG（Boro-Phospho Silicate Glass）膜等の層間絶縁膜を成膜してリフローを施し、その表面にCMP（ChemicalMechanical Polishing）法による研磨やエッチバックを施すという方法がある。

【0003】

【発明が解決しようとする課題】しかしながら、CMP法による平坦化は、半導体基板面内或いは半導体基板間において層間絶縁膜の研磨均一性や再現性に劣り、研磨残膜の膜厚のバラツキが大きい。このため、平坦化後のフォトリソグラフィー工程において、下層に存する層間絶縁膜の膜厚のバラツキにより反射率が変動し、再現性よく配線やコンタクト孔のパターニングを行うことができないという問題がある。また、層間絶縁膜にリフローを施し、表面をエッチバックする方法では、リフローが終了した時点ではさほど平坦化が得られない以上、メモリセル部分と周辺回路部分とのグローバル段差を解消することは困難である。

【0004】以下、CMPやエッチバックを用いた平坦化法のいくつかの具体例を以下に示す。

【0005】先ず、特開平7-99195号公報には、メモリセル部と周辺回路部を覆い、表面が平坦化されるように塗布膜を形成し、メモリセル部の上部に不純物が到達するようにイオン注入を施し、ウェットエッチング（ドライエッチングや研磨でもよい。）により塗布膜とともにメモリセル部の不純物注入層を除去する方法が開示されている。この方法によれば、メモリセル部と周辺回路部との段差をある程度は緩和させることができるものの、十分な平坦化は得られず、しかもイオン注入工程が増加するなどの不都合が招来される。

【0006】次に、特開平7-297187号公報には、配線を覆うようにシリコン酸化膜を形成した後、更にシリコン窒化膜を堆積し、シリコン窒化膜が残るようにその表層を研磨除去して、しかる後、シリコン酸化膜が一部残り且つシリコン窒化膜が除去されるようにエッチバックを施す方法が開示されている。この方法においては、当然のことながらシリコン酸化膜とシリコン窒化膜のエッチング速度は大きく異なるため、1層の配線のような膜厚の薄いものであればある程度の平坦化は得られるものの、メモリセル部と周辺回路部との間の如く大きな段差を緩和させることはできない。

4

【0007】次に、特開平8-15882号公報には、各種配線等を覆うように層間絶縁膜を形成した後、表面を研磨して平坦化する方法が開示されているが、この方法については、既述したように研磨均一性や再現性に劣り、研磨残膜の膜厚のバラツキが大きいという問題がある。

【0008】次に、特開平8-227935号公報には、素子分離用絶縁膜をトレンチ（溝）内に絶縁膜を充填したものとし、この溝部を形成するために形成されたシリコン窒化膜をストッパーとしてCMPを施す方法が開示されている。この方法によれば、素子分離用絶縁膜のボイドを除去して集積度の高い半導体装置が得られるとされているが、そもそもこの方法はトレンチ型の素子分離構造に適用が限定されるものである。

【0009】そこで、本発明の目的は、例えばDRAMのようにメモリセル部と周辺回路部との間に大きさ段差を有する半導体装置において、簡便な手法により十分な平坦化を得ることができ、更なる高集積化の実現を可能とする半導体装置及びその製造方法を提供することである。

【0010】

【課題を解決するための手段】本発明の半導体装置の製造方法は、半導体基板上の素子分離領域に素子分離構造を形成する第1の工程と、上記素子分離構造により囲まれて画定された素子形成領域を含む上記半導体基板上に半導体素子を形成する第2の工程と、前記半導体素子上を含む前記半導体基板の全面を覆うように第1の絶縁膜を形成する第3の工程と、前記半導体素子を埋め込むように、前記第1の絶縁膜上に当該第1の絶縁膜に比して厚い第2の絶縁膜を形成する第4の工程と、前記第1の絶縁膜上に前記第2の絶縁膜が残り且つ前記第2の絶縁膜の表面が平坦化されるように前記第2の絶縁膜を研磨する第5の工程と、前記第1の絶縁膜の一部が最初に露出するまで前記第2の絶縁膜の全面をエッチバックし、前記第2の絶縁膜の表面を平坦化する第6の工程とを有する。

【0011】本発明の半導体装置の製造方法の一態様例においては、前記半導体素子が、メモリセルを構成する第1の素子と、前記メモリセルの周辺回路部を構成する第2の素子とからなる。

【0012】本発明の半導体装置の製造方法の一態様例においては、前記第1の絶縁膜がシリコン酸化膜又はシリコン窒化膜からなる。

【0013】本発明の半導体装置の製造方法の一態様例は、前記第6の工程の後に、前記第2の絶縁膜上に第3の絶縁膜を形成する第7の工程を更に有する。

【0014】本発明の半導体装置の製造方法は、半導体基板上の素子分離領域に素子分離構造を形成する第1の

5

工程と、上記素子分離構造により囲まれて画定された素子形成領域を含む上記半導体基板上に半導体素子を形成する第2の工程と、前記半導体素子を埋め込むように層間絶縁膜を形成する第3の工程と、前記半導体素子上に前記層間絶縁膜が残り且つ前記層間絶縁膜の表面が平坦化されるように前記層間絶縁膜を研磨する第4の工程と、前記層間絶縁膜内に埋め込まれた前記半導体素子の構成要素となる各導電膜のうち、最上層の前記導電膜上に形成されたキャップ絶縁膜の一部が最初に露出するまで前記層間絶縁膜の全面をエッチバックし、前記層間絶縁膜の表面を平坦化する第5の工程とを有する。

【0015】本発明の半導体装置の製造方法の一態様例においては、前記半導体素子が、メモリセルを構成する第1の素子と、前記メモリセルの周辺回路部を構成する第2の素子とからなる。

【0016】本発明の半導体装置の製造方法の一態様例においては、前記最上層の前記導電膜上に形成された前記キャップ絶縁膜がシリコン酸化膜又はシリコン窒化膜からなる。

【0017】本発明の半導体装置の製造方法の一態様例は、前記第5の工程の後に、前記層間絶縁膜上に上層絶縁膜を形成する第6の工程を更に有する。

【0018】本発明の半導体装置は、素子分離構造により囲まれて画定された素子形成領域を含む半導体基板上に半導体素子が形成されてなる半導体装置であって、前記半導体素子上を含む前記半導体基板の全面を覆うように形成された第1の絶縁膜と、前記半導体素子を埋め込むように、前記第1の絶縁膜上に当該第1の絶縁膜に比して厚く形成された第2の絶縁膜とを備え、前記第2の絶縁膜の表面には少なくとも前記第1の絶縁膜の最上部に位置する一部位が露出しているとともに、前記第2の絶縁膜の前記表面が平坦化されている。

【0019】本発明の半導体装置の一態様例においては、前記半導体素子が、メモリセルを構成する第1の素子と、前記メモリセルの周辺回路部を構成する第2の素子とからなる。

【0020】本発明の半導体装置の一態様例においては、前記第1の絶縁膜がシリコン酸化膜又はシリコン窒化膜からなる。

【0021】本発明の半導体装置は、素子分離構造により囲まれて画定された素子形成領域を含む半導体基板上に半導体素子が形成されてなる半導体装置であって、前記半導体素子を埋め込むように形成された層間絶縁膜を備え、前記層間絶縁膜の表面には、前記半導体素子の構成要素となる各導電膜のうち、最上層の前記導電膜上に形成されたキャップ絶縁膜の一部位が露出しているとともに、前記層間絶縁膜の前記表面が平坦化されている。

【0022】本発明の半導体装置の一態様例においては、前記半導体素子が、メモリセルを構成する第1の素子と、前記メモリセルの周辺回路部を構成する第2の素子とからなる。

6

【0023】本発明の半導体装置の一態様例においては、前記最上層の前記導電膜上に形成された前記キャップ絶縁膜がシリコン酸化膜又はシリコン窒化膜からなる。

【0024】

【作用】半導体装置を製造するに際して、その層間絶縁膜の平坦化法の有力な手法としては、研磨法とエッチバック法がある。研磨法はグローバル段差の解消には優れている反面、研磨均一性に若干劣る。一方、エッチバック法は研磨均一性に優れ、終点判定も容易であるため再現性が良好である反面、層間絶縁膜の堆積後の段差を反映するためにグローバル段差の解消には不適である。本発明は、これら2つの平坦化法を併用し、互いの短所を補うと共に長所のみを半導体装置の製造方法に適用するものである。

【0025】即ち、本発明の半導体装置の製造方法においては、先ず、半導体素子を埋め込む第2の絶縁膜（層間絶縁膜）の表面を研磨する。このとき、第2の絶縁膜（層間絶縁膜）の表面を十分に平坦化することはでき、グローバル段差の低減は良好になされる。しかしながら、半導体基板面内或いは半導体基板間における層間絶縁膜等の研磨均一性や再現性に劣り、研磨量のばらつき（層間絶縁膜の残膜）が大きい。続いて、ある程度平坦化された第2の絶縁膜（層間絶縁膜）の表面をエッチバックする。このとき、第2の絶縁膜（層間絶縁膜）に埋め込まれた半導体素子を覆う第1の絶縁膜の一部や、半導体素子の構成要素となる各導電膜のうち、最上層の前記導電膜上に形成されたキャップ絶縁膜の一部が最初に露出するまで、即ち第1の絶縁膜の一部或いはキャップ絶縁膜の一部をストッパーとしてエッチバックが施されるため、エッチバックの終了時点が確実に規定される。従って、研磨に続くエッチバックにより、第2の絶縁膜（層間絶縁膜）が最終的に極めて高い精度をもって平坦化されることになる。

【0026】

【発明の実施の形態】以下、本発明を適用したいくつかの具体的な実施の形態について、図面を参照しながら詳細に説明する。

【0027】（第1の実施形態）初めに、第1の実施形態について説明する。この第1の実施形態においては、半導体装置としてDRAMを例示し、その構成を製造方法とともに説明する。なお、第1の実施形態では、メモリキャパシタがビット配線の上層に位置する、いわゆるCOB（Capacitor Over Bitline）構造のDRAMを例にとって説明する。

【0028】先ず、図1（a）に示すように、p型のシリコン半導体基板1の上に、いわゆるフィールドシールド素子分離法により素子分離領域にフィールドシールド素子分離構造22を形成して素子形成領域21を画定す

る。

【００２９】即ち、先ずｐ型のシリコン半導体基板１の上に、シリコン酸化膜２、多結晶シリコン膜３及びシリコン酸化膜４を、それぞれ膜厚を例えば５０ｎｍ，２００ｎｍ，２００ｎｍ程度に順次形成する。続いて、これらシリコン酸化膜２、多結晶シリコン膜３及びシリコン酸化膜４をフォトリソグラフィー及びそれに続くドライエッチング等によりパターニングしてそれぞれ選択的に除去して素子形成領域２１を画定する。そして、残存したシリコン酸化膜２、多結晶シリコン膜３及びシリコン酸化膜４を覆うように全面にシリコン酸化膜を成膜した後に、当該シリコン酸化膜の全面をＲＩＥ等により異方性ドライエッチングしてシリコン酸化膜２、多結晶シリコン膜３及びシリコン酸化膜４の側壁にのみシリコン酸化膜を残し、側壁保護膜５を形成する。これにより、フィールド領域に、シリコン酸化膜により囲まれた多結晶シリコン膜からなるシールドプレート電極を備えたフィールドシールド素子分離構造２２が形成される。

【００３０】次に、図１（ｂ）に示すように、フィールドシールド素子分離構造２２により互いに分離されて相対的に画定された素子形成領域２１上のシリコン半導体基板１の表面に熱酸化を施して膜厚１５ｎｍ程度のゲート酸化膜６を形成する。続いて、フィールドシールド素子分離構造２２を含む全面にＣＶＤ法により多結晶シリコン膜及びシリコン酸化膜を順次成膜する。次いで、これらシリコン酸化膜及び多結晶シリコン膜をパターニングして、フィールドシールド素子分離構造２２上を跨いで素子形成領域２１上に帯状にシリコン酸化膜からなるキャップ絶縁膜７及び多結晶シリコン膜からなるゲート電極８を形成する。

【００３１】続いて、素子形成領域２１上及びフィールドシールド素子分離構造２２上の各キャップ絶縁膜７を覆うようにＣＶＤ法により全面にシリコン酸化膜を堆積形成し、続いて当該シリコン酸化膜の全面をＲＩＥ等により異方性ドライエッチングして、素子形成領域２１におけるゲート電極８間のゲート酸化膜６を除去するとともに各ゲート電極８の側壁にのみ上記シリコン酸化膜を残して側壁保護膜９を形成する。このとき、フィールドシールド素子分離構造２２上を跨ぐように素子形成領域２１上にゲート絶縁膜６を介して帯状にパターン形成されたゲート電極８を有し、このゲート電極８を覆うようにキャップ絶縁膜７及び側壁保護膜９が形成されてなるゲート電極構造２３が完成する。

【００３２】次に、図１（ｃ）に示すように、ＣＶＤ法によりｎ型不純物、例えばリン（Ｐ）がドープされてなる多結晶シリコン膜をフィールドシールド素子分離構造２２上を含む全面に堆積形成する。このとき、多結晶シリコン膜からシリコン半導体基板１の素子形成領域２１におけるゲート電極８の両側に当該多結晶シリコン膜内のリン（Ｐ）が拡散し、ソース／ドレインとなる各拡散層１０が形成される。

【００３３】続いて、多結晶シリコン膜を素子形成領域２１上においてキャップ絶縁膜７上で分断されるように島状にパターニングし、各拡散層１０と各々独立に接続されるようにパッド多結晶シリコン膜１１を形成する。各パッド多結晶シリコン膜１１は、その端部がゲート電極構造２３上の一部を覆うような島状に形成されることになる。

【００３４】次に、図２（ａ）に示すように、減圧ＣＶＤ法によりシリコン酸化膜（ＳｉＯｘ膜）からなる層間絶縁膜１２を膜厚１００ｎｍ程度に堆積形成する。続いて、層間絶縁膜１２を覆うように常圧ＣＶＤ法によりＢＰＳＧ膜からなる層間絶縁膜１３を膜厚６００ｎｍ程度に堆積形成し、リフローを施した後、層間絶縁膜１３の表層部位を化学機械研磨（Chemical Mechanical Polishing ；ＣＭＰ）法により膜厚１００～２００ｎｍ程度だけ研磨除去する。

【００３５】次に、図２（ｂ）に示すように、ＣＭＰ法によりある程度表面が平坦化された層間絶縁膜１３に今度はドライエッチング法により全面エッチバック処理を施す。エッチング条件としては、例えば平行平板型エッチング装置を用いて、エッチングガスをＣＨＦ３（６０ｓｃｃｍ），ＣＦ４（６０ｓｃｃｍ），Ａｒ（８００ｓｃｃｍ）の混合ガスとし、エッチング圧力を１７００ｍＴｏｒｒ、投入パワーをＲＦ電力で７５０Ｗとする。ここで、エッチバック処理により層間絶縁膜１３のエッチングが進むと、やがて層間絶縁膜１３の下層に存する層間絶縁膜１２の最上部位、ここではフィールドシールド素子分離構造２２上に位置するゲート電極構造２３上にかかるパッド多結晶シリコン膜１１を覆う部位の層間絶縁膜１２が露出する。このとき、層間絶縁膜１３のエッチング面積が減少し、それに伴ってプラズマ中のＣＯ発光スペクトル強度も減少する。本実施形態では、このＣＯ発光スペクトル強度の変化量を検出し、層間絶縁膜１２が露出した時点をエッチングの終点に規定する。なお、実際には当該時点にエッチングを終了しても、層間絶縁膜１２は膜厚が薄いためにパッド多結晶シリコン膜１１の最上部位が若干露出することになる。本実施形態においては、ＣＭＰ法による表面研磨に続く前記エッチバック処理により、層間絶縁膜１３を再現性良くほぼ最小膜厚にて全面を十分に平坦化することができる。

【００３６】次に、図３（ａ）に示すように、平坦化された層間絶縁膜１３上に減圧ＣＶＤ法によりＳｉＯｘ膜からなる層間絶縁膜１４を膜厚１００ｎｍ程度に堆積形成する。続いて、層間絶縁膜１４，１３，１２をパターニングして、パッド多結晶シリコン膜１１（図中、中央部位のパッド多結晶シリコン膜１１）の表面の一部を露出させるビットコンタクト孔１５を形成する。

【００３７】次に、図３（ｂ）に示すように、ビットコンタクト孔１５の内壁面を含む層間絶縁膜１４の全面に

9

減圧ＣＶＤ法によりｎ型不純物、例えばリンをドープした多結晶シリコン膜１６を膜厚６０ｎｍ程度に形成する。続いて、多結晶シリコン膜１６上にスパッタ法又はＣＶＤ法によりタングステンシリサイド膜１７を膜厚２００ｎｍ程度に形成する。そして、タングステンシリサイド膜１７及び多結晶シリコン膜１６をパターニングして、帯状のビット配線２４を形成する。

【００３８】しかる後、図示は省略したが、層間絶縁膜やコンタクト孔、メモリキャパシタの形成、それに続く金属配線の形成等の工程を経て、ＤＲＡＭを完成させる。

【００３９】上述のように、第１の実施形態においては、先ず、ゲート電極構造２３やパッド多結晶シリコン膜１１を層間絶縁膜１２を介して埋め込む層間絶縁膜１３の表面を研磨する。このとき、層間絶縁膜１３の表面を十分に平坦化することはでき、グローバル段差の低減は良好になされる。しかしながら、シリコン半導体基板１の面内或いはシリコン半導体基板１間における層間絶縁膜１３の研磨均一性や再現性に劣り、研磨量のばらつき（層間絶縁膜１３の残膜）が大きい。続いて、ある程度平坦化された層間絶縁膜１３の表面をエッチバックする。このとき、層間絶縁膜１３の下層に形成された層間絶縁膜１２の最上層部位が最初に露出するまで、即ち層間絶縁膜１２の一部をストッパーとしてエッチバックが施されるため、エッチバックの終了時点が確実に規定される。従って、研磨に続くエッチバックにより、層間絶縁膜１３が最終的に極めて高い精度をもって平坦化されることになる。

【００４０】従って、第１の実施形態によれば、メモリセル領域と周辺回路領域との間に大きさ段差を有するＤＲＡＭにおいて、簡便な手法により十分な平坦化を得ることができ、更なる高集積化の実現が可能となる。

【００４１】－変形例－

ここで、第１の実施形態の変形例について説明する。この変形例においては、第１の実施形態とほぼ同様の工程を経てＤＲＡＭを製造するが、層間絶縁膜１２をＳｉＯｘ膜を材料とする代わりにシリコン窒化膜（Si_3N_4膜）から形成する。

【００４２】このように、Si_3N_4膜からなる層間絶縁膜１２を形成することにより、上述した第１の実施形態の効果に加えて、Si_3N_4膜はＳｉＯｘ膜に比してエッチング速度が低いため、エッチバック処理時において層間絶縁膜１２がより正確にストッパーとして機能し、更に確実に層間絶縁膜１３の平坦化を行うことができる。

【００４３】（第２の実施形態）続いて、本発明の第２の実施形態について説明する。ここでは、第１の実施形態と同様にＤＲＡＭの構成をその製造方法とともに例示する。図４～図９は第２の実施形態のＤＲＡＭの製造方法の主要工程を示す概略断面図であり、図４（ａ）～図４（ｃ）及び図５（ａ），図６（ａ），図７（ａ），図８（ａ），図９（ａ）がビット配線の長手方向に沿った図、図５（ｂ），図６（ｂ），図７（ｂ），図８（ｂ），図９（ｂ）が長手方向に直交する方向に沿った図である。なお、第１の実施形態のＤＲＡＭの構成要素と同一の部位には同符号を付す。

10

【００４４】この第２の実施形態においては、先ず第１の実施形態の場合と同様に、図１（ａ）～図１１（ｂ）の工程を経て、フィールドシールド層間絶縁膜２２やゲート電極構造２３を形成する。ここで、後にメモリキャパシタ等が形成される素子形成領域２１をメモリセル領域２１ａとし、このメモリセルに隣接する他の素子形成領域２１を周辺回路領域２１ｂとする。この周辺回路領域２１ｂには、メモリセル領域２１ａにおけるゲート電極構造２３と同時にゲート電極構造３１を形成する。

【００４５】次に、図４（ａ）に示すように、メモリセル領域２１ａ上及び周辺回路領域２１ｂ上を含む全面に、ＣＶＤ法によりｎ型不純物、例えばリン（Ｐ）がドープされてなる多結晶シリコン膜を堆積形成する。このとき、多結晶シリコン膜からシリコン半導体基板１のメモリセル領域２１ａ及び周辺回路領域２１ｂにおけるゲート電極８の両側に当該多結晶シリコン膜内のリン（Ｐ）が拡散し、メモリセル領域２１ａにはソース，ドレインとなる各拡散層１０が、周辺回路領域２１ｂにはソース，ドレインとなる各拡散層３３がそれぞれ形成される。

【００４６】続いて、多結晶シリコン膜をメモリセル領域２１ａ及び周辺回路領域２１ｂにおいてそれぞれキャップ絶縁膜７上で分断されるように島状にパターニングし、メモリセル領域２１ａには各拡散層１０と各々独立に接続されるようにパッド多結晶シリコン膜１１を、周辺回路領域２１ｂには各拡散層３３と各々独立に接続されるようにパッド多結晶シリコン膜３２をそれぞれ形成する。各パッド多結晶シリコン膜１１，３２は、その端部がゲート電極構造２３，３１上の一部を覆うような島状に形成されることになる。

【００４７】次に、図４（ｂ）に示すように、メモリセル領域２１ａ上及び周辺回路領域２１ｂ上を含む全面にＣＶＤ法によりＳｉＯｘ膜よりなる層間絶縁膜２５を形成した後、この層間絶縁膜２５をパターニングして、パッド多結晶シリコン膜１１（図中、メモリセル領域２１ａにおける中央部位のパッド多結晶シリコン膜１１）の表面の一部を露出させるビットコンタクト孔１５を形成する。

【００４８】次に、図４（ｃ）に示すように、メモリセル領域２１ａにおいて、ビットコンタクト孔１５の内壁面を含む層間絶縁膜２５の全面に減圧ＣＶＤ法によりｎ型不純物、例えばリンをドープした多結晶シリコン膜１６を膜厚６０ｎｍ程度に形成する。続いて、多結晶シリコン膜１６上にスパッタ法又はＣＶＤ法によりタングス

テンシリサイド膜17を膜厚200nm程度に、更にタングステンシリサイド膜17上にシリコン窒化膜（Si_3N_4膜）18を順次形成する。そして、Si_3N_4膜18、タングステンシリサイド膜17及び多結晶シリコン膜16をパターニングして、帯状のビット配線24を形成する。ここで、Si_3N_4膜18はビット配線24のキャップ絶縁膜となる。

【0049】続いて、図5（a）及び図5（b）に示すように、メモリセル領域21a上及び周辺回路領域21b上を含む全面にCVD法によりSi_3N_4膜を形成し、このSi_3N_4膜の全面を異方性エッチングして、ビット配線24及びキャップ絶縁膜18の側面に側壁保護膜43を形成する。なお、図5（b）はビット配線24の長手方向に直交する方向の断面を示しており、図5（a）の破線A－A'の一に対応した断面図である。このことは、以下の図6～図9においても同様である。

【0050】次に、図6（a）及び図6（b）に示すように、メモリセル領域21a上及び周辺回路領域21b上を含む全面に常圧CVD法によりBPSG膜からなる層間絶縁膜44を膜厚10000Å程度に堆積形成し、リフローを施した後、層間絶縁膜44の表層部位をCMP法により膜厚100～200nm程度だけ研磨除去する。

【0051】次に、図7（a）及び図7（b）に示すように、CMP法によりある程度表面が平坦化された層間絶縁膜44に今度はドライエッチング法により全面エッチバック処理を施す。エッチング条件としては、例えば平行平板型エッチング装置を用いて、エッチングガスをCHF_3（60sccm），CF_4（60sccm），Ar（800sccm）の混合ガスとし、エッチング圧力を1700mTorr，投入パワーをRF電力で750Wとする。ここで、エッチバック処理により層間絶縁膜44のエッチングが進むと、やがて層間絶縁膜44の下層に存するビット配線24のキャップ絶縁膜18の表面が露出する。このとき、層間絶縁膜44のエッチング面積が減少し、それに伴ってプラズマ中のCO発光スペクトル強度も減少する。本実施形態では、このCO発光スペクトル強度の変化量を検出し、キャップ絶縁膜18が露出した時点をエッチングの終点に規定する。本実施形態においては、CMP法による表面研磨に続く前記エッチバック処理により、層間絶縁膜44を再現性良くほぼ最小膜厚にて全面を十分に平坦化することができる。

【0052】次に、図8（a）及び図8（b）に示すように、ビット配線24及びキャップ絶縁膜18を覆うように全面に減圧CVD法によりSiO_x膜からなる層間絶縁膜34を膜厚200nm程度に形成した後、図示は省略するが、層間絶縁膜34，44，25をパターニングして、パッド多結晶シリコン膜11（図中、メモリセル領域21aにおける両端部位のパッド多結晶シリコン膜11）の表面の一部を露出させるストレージコンタクト孔を形成する。続いて、ストレージコンタクト孔内を含む全面に減圧CVD法によりn型不純物、例えばリンをドープした多結晶シリコン膜を膜厚460nm程度に形成する。続いて、多結晶シリコン膜をパターニングして、ストレージコンタクト孔を通じてパッド多結晶シリコン膜11と接続してなるストレージノード電極35を形成する。続いて、ストレージノード電極35を覆うように酸化膜、窒化膜及び酸化膜の3層構造となる誘電体膜36を形成した後、減圧CVD法によりn型不純物、例えばリンをドープした多結晶シリコン膜を膜厚150nm程度に形成する。続いて、多結晶シリコン膜及び誘電体膜36をパターニングして、セルプレート電極37を形成する。このとき、ストレージノード電極35とセルプレート電極37とが誘電体膜36を介して対向して容量結合するメモリキャパシタが完成する。

【0053】次に、図9（a）及び図9（b）に示すように、メモリキャパシタを覆うように、メモリセル領域21a上及び周辺回路領域21b上を含む全面にCVD法によりSiO_x膜を膜厚100nm程度に形成した後、続いて常圧CVD法によりBPSG膜を膜厚500nm程度に形成し、合計膜厚が600nm程度の層間絶縁膜38を形成する。続いて、周辺回路領域21bにおいてゲート電極8と通じるコンタクト孔（図示は省略する）を形成する。

【0054】しかる後、図示は省略したが、層間絶縁膜や接続孔の形成、それに続く金属配線の形成等の工程を経て、DRAMを完成させる。

【0055】上述のように、第2の実施形態においては、先ず、メモリキャパシタ等を埋め込む層間絶縁膜44の表面を研磨する。このとき、層間絶縁膜44の表面を十分に平坦化することはでき、グローバル段差の低減は良好になされる。しかしながら、シリコン半導体基板1の面内或いはシリコン半導体基板1間における層間絶縁膜44の研磨均一性や再現性に劣り、研磨量のばらつき（層間絶縁膜44の残膜）が大きい。続いて、ある程度平坦化された層間絶縁膜44の表面をエッチバックする。このとき、層間絶縁膜44の下層に位置するキャップ絶縁膜18の表面が最初に露出するまで、即ちキャップ絶縁膜18をストッパーとしてエッチバックが施されるため、エッチバックの終了時点が確実に規定される。従って、研磨に続くエッチバックにより、層間絶縁膜44がメモリセル領域21a上から周辺回路領域21b上にかけて最終的に極めて高い精度をもって平坦化されることになる。

【0056】従って、第2の実施形態によれば、メモリセル領域21aと周辺回路領域21bとの間に大きさ段差を有するDRAMにおいて、簡便な手法により十分な平坦化を得ることができ、更なる高集積化の実現が可能となる。

【0057】（第3の実施形態）続いて、本発明の第3

の実施形態について説明する。ここでは、半導体装置としてMOSトランジスタを例示し、その構成を製造方法とともに説明する。なお、第1の実施形態のDRAMの構成要素と同一の部位には同符号を付す。

【0058】この第3の実施形態においては、先ず第1の実施形態の場合と同様に、図1（a）の工程を経て、フィールドシールド層間絶縁膜22を形成してシリコン半導体基板1上に素子形成領域21を画定する。

【0059】次に、図10（a）に示すように、素子形成領域21上のシリコン半導体基板1の表面に熱酸化を施して膜厚110nm程度のゲート酸化膜6を形成する。続いて、フィールドシールド素子分離構造22を含む全面にCVD法により多結晶シリコン膜及びSi_3N_4膜を膜厚がそれぞれ200～300nm程度及び20～50nm程度となるように順次成膜する。次いで、これらSi_3N_4膜及び多結晶シリコン膜をパターニングして、フィールドシールド素子分離構造22上を跨いで素子形成領域21上に帯状にSi_3N_4膜からなるキャップ絶縁膜51及び多結晶シリコン膜からなるゲート電極8を形成する。

【0060】続いて、全面にCVD法によりシリコン酸化膜を形成し、このシリコン酸化膜の全面を異方性エッチングして、各ゲート電極8及びキャップ絶縁膜51の側面に側壁保護膜52を形成し、ゲート電極構造53を形成する。

【0061】次に、図10（b）に示すように、CVD法により全面を覆うようにシリコン酸化膜55を膜厚100nm程度に形成した後、常圧CVD法によりBPSG膜54を、素子形成領域21上のゲート電極構造53が埋め込まれる膜厚、ここでは600nm程度に形成し、リフローを施した後、層間絶縁膜54の表層部位をCMP法により膜厚100～200nm程度だけ研磨除去する。

【0062】次に、図10（c）に示すように、CMP法によりある程度表面が平坦化された層間絶縁膜54に今度はドライエッチング法により全面エッチバック処理を施す。エッチング条件としては、例えば平行平板型エッチング装置を用いて、エッチングガスをCHF_3（60sccm），CF_4（60sccm），Ar（800sccm）の混合ガスとし、エッチング圧力を1700mTorr、投入パワーをRF電力で750Wとする。ここで、エッチバック処理により層間絶縁膜54のエッチングが進むと、やがて層間絶縁膜54の下層のフィールドシールド素子分離構造22上に存するゲート電極構造53のキャップ絶縁膜51の表面が露出する。このとき、層間絶縁膜54のエッチング面積が減少し、それに伴ってプラズマ中のCO発光スペクトル強度も減少する。本実施形態では、このCO発光スペクトル強度の変化量を検出し、キャップ絶縁膜52が露出した時点をエッチングの終点に規定する。本実施形態においては、CMP法による表面研磨に続く前記エッチバック処理により、層間絶縁膜54を再現性良くほぼ最小膜厚にて全面を十分に平坦化することができる。

【0063】しかる後、図示は省略したが、メモリセルキャパシタや層間絶縁膜及び接続孔の形成、それに続く金属配線の形成等の工程を経て、MOSトランジスタを完成させる。

【0064】上述のように、第3の実施形態においては、先ず、ゲート電極構造53を埋め込む層間絶縁膜54の表面を研磨する。このとき、続いて、ある程度平坦化された層間絶縁膜54の表面をエッチバックする。このとき、層間絶縁膜54の表面を十分に平坦化することはでき、グローバル段差の低減は良好になされる。しかしながら、シリコン半導体基板1の面内或いはシリコン半導体基板1間における層間絶縁膜54の研磨均一性や再現性に劣り、研磨量のばらつき（層間絶縁膜54の残膜）が大きい。層間絶縁膜54の下層に位置するキャップ絶縁膜51の表面が最初に露出するまで、即ちキャップ絶縁膜51をストッパーとしてエッチバックが施されるため、エッチバックの終了時点が確実に規定される。従って、研磨に続くエッチバックにより、層間絶縁膜54が最終的に極めて高い精度をもって平坦化されることになる。

【0065】なお、本発明は、上述の第1～第3の実施形態及に限定されるものではない。例えば、素子分離構造をフィールドシールド素子分離法によりフィールドシールド素子分離構造として形成する代わりに、いわゆるLOCOS法によりフィールド酸化膜として形成したり、トレンチ分離法によりシリコン半導体基板に溝を形成し、この溝内を絶縁膜で埋め込んでトレンチ型素子分離構造を形成してもよい。

【0066】

【発明の効果】本発明によれば、例えばメモリセル領域と周辺回路領域との間に大きさ段差を有するDRAMや段差の大きなMOSトランジスタ等において、簡便な手法により十分な平坦化を得ることができ、更なる高集積化の実現が可能となる。

【図面の簡単な説明】

【図1】本発明の第1の実施形態において、DRAMの製造方法を工程順に示す概略断面図である。

【図2】図1に引き続き、本発明の第1の実施形態において、DRAMの製造方法を工程順に示す概略断面図である。

【図3】図2に引き続き、本発明の第1の実施形態において、DRAMの製造方法を工程順に示す概略断面図である。

【図4】本発明の第2の実施形態において、DRAMの製造方法を工程順に示す概略断面図である。

【図5】図1に引き続き、本発明の第2の実施形態において、DRAMの製造方法を工程順に示す概略断面図で

15

ある。

【図6】図5に引き続き、本発明の第2の実施形態において、DRAMの製造方法を工程順に示す概略断面図である。

【図7】図6に引き続き、本発明の第2の実施形態において、DRAMの製造方法を工程順に示す概略断面図である。

【図8】図7に引き続き、本発明の第2の実施形態において、DRAMの製造方法を工程順に示す概略断面図である。

【図9】図8に引き続き、本発明の第2の実施形態において、DRAMの製造方法を工程順に示す概略断面図である。

【図10】本発明の第3の実施形態において、MOSトランジスタの製造方法を工程順に示す概略断面図である。

【符号の説明】

1　p型のシリコン半導体基板

6　ゲート絶縁膜

7，42，51　キャップ絶縁膜

16

8　ゲート電極

9　（シリコン酸化膜からなる）側壁保護膜

10，33　拡散層

11，32　多結晶シリコンパッド

12，13，14，25，34，38，44，54　層間絶縁膜

15　ビットコンタクト孔

16　多結晶シリコン膜

17　タングステンシリサイド膜

18　シリコン窒化膜

21　素子形成領域

21a　メモリセル領域

21b　周辺回路領域

22　フィールドシールド素子分離構造

23，31，53　ゲート電極構造

24　ビット配線

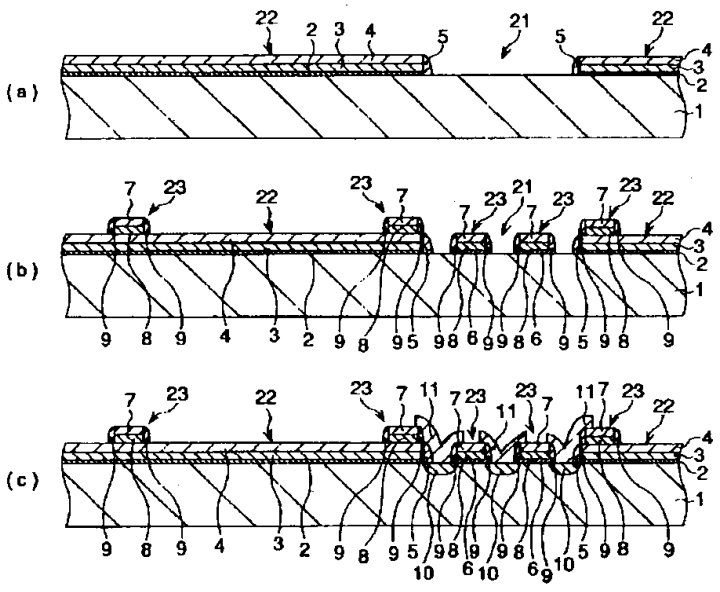
35　ストレージノード電極

36　誘電体膜

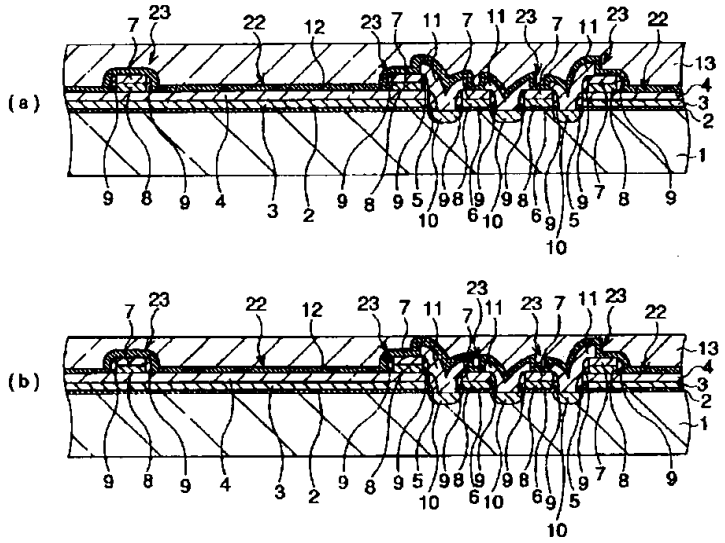
37　セルプレート電極

43，52　（シリコン窒化膜からなる）側壁保護膜

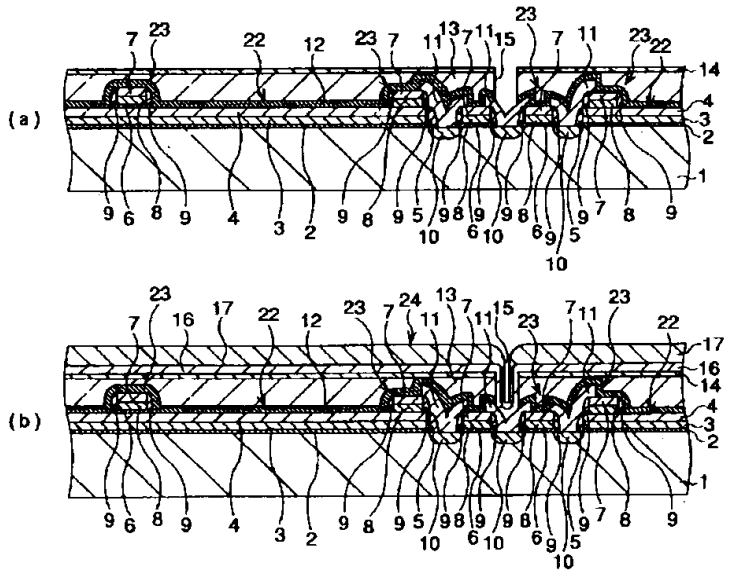
【図1】



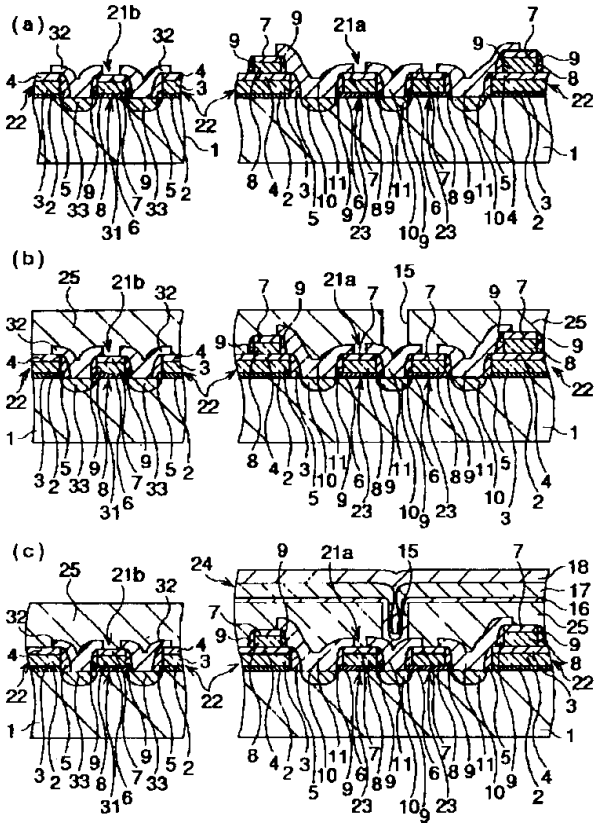
【図2】



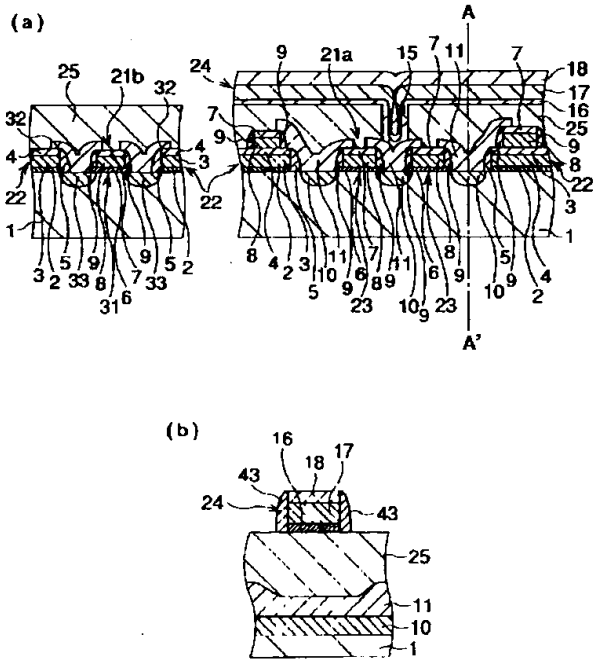
【図3】



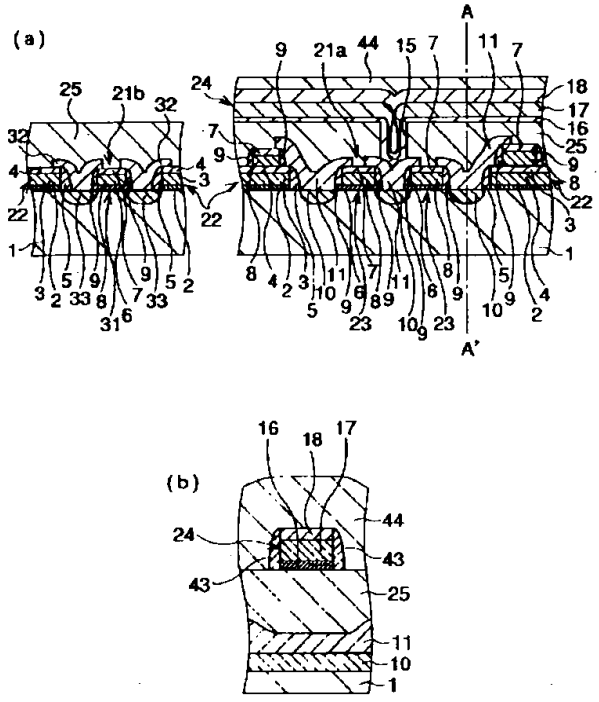
【図1】



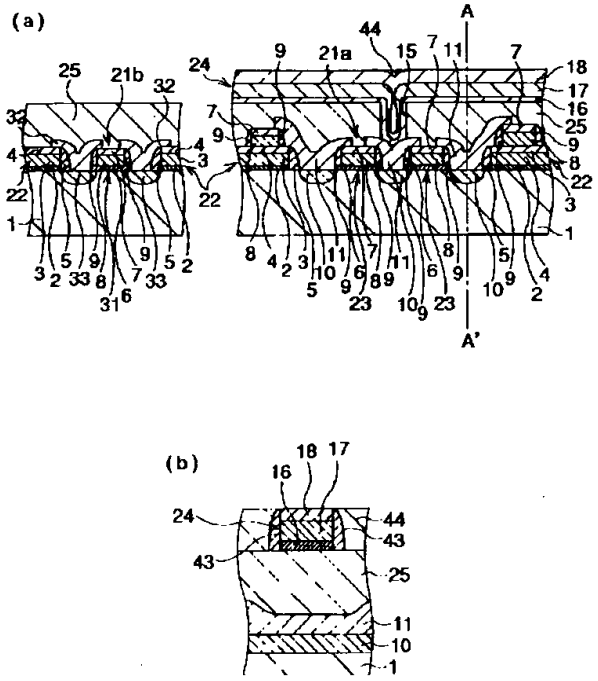
【図5】



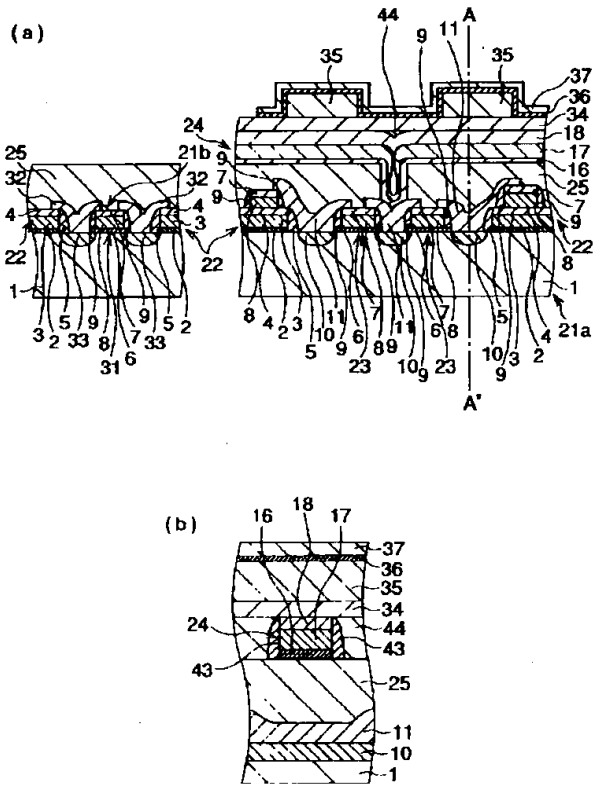
【図6】



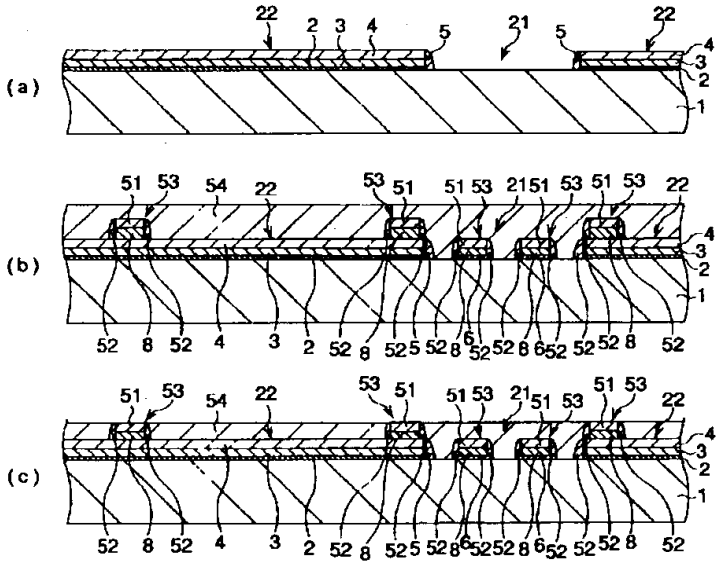
【図7】



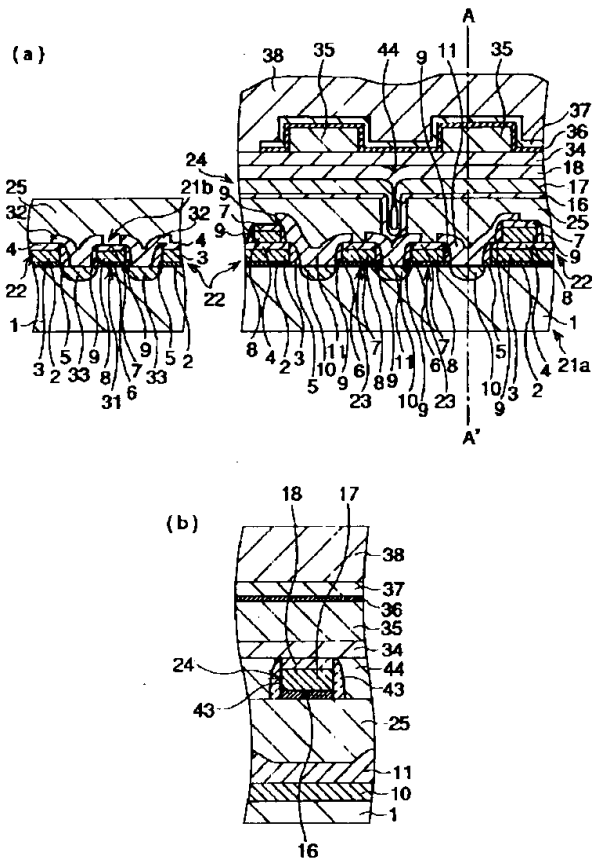
【図8】



【図10】



【図9】


(a)
A
A'
38
35
44
9
11
35
37
36
34
18
17
16
25
7
9
22
8
1
21a
24
21b
32
4
3
22
5
2
33
6
31
(b)
18
17
38
37
36
35
34
44
43
25
11
10
1
16
24

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

JP 11-177,058

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The manufacture method of a semiconductor device characterized by providing the following. The 1st process which forms isolation structure in the isolation field on a semiconductor substrate. The 2nd process which forms a semiconductor device on the above-mentioned semiconductor substrate including the element formation field which was surrounded by the above-mentioned isolation structure and demarcated. The 3rd process which forms the 1st insulator layer so that the whole surface of the aforementioned semiconductor substrate including the aforementioned semiconductor device top may be worn. The 4th process which forms the 2nd thick insulator layer as compared with the 1st insulator layer concerned on the insulator layer of the above 1st so that the aforementioned semiconductor device may be embedded, The 5th process which grinds the 2nd insulator layer of the above so that the 2nd insulator layer of the above may remain on the insulator layer of the above 1st and flattening of the front face of the 2nd insulator layer of the above may be carried out, The 6th process which carries out etchback of the whole surface of the 2nd insulator layer of the above until a part of 1st insulator layer of the above is exposed first, and carries out flattening of the front face of the 2nd insulator layer of the above.

[Claim 2] The manufacture method of a semiconductor device according to claim 1 that the aforementioned semiconductor device is characterized by the bird clapper from the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell.

[Claim 3] The manufacture method of a semiconductor device according to claim 1 or 2 that the 1st insulator layer of the above is characterized by the bird clapper from a silicon oxide or a silicon nitride.

[Claim 4] The manufacture method of a semiconductor device given in any 1 term of the claims 1-3 characterized by having further the 7th process which forms the 3rd insulator layer on the insulator layer of the above 2nd after the 6th process of the above.

[Claim 5] The manufacture method of a semiconductor device characterized by providing the following. The 1st process which forms isolation structure in the isolation field on a semiconductor substrate. The 2nd process which forms a semiconductor device on the above-mentioned semiconductor substrate including the element formation field which was surrounded by the above-mentioned isolation structure and demarcated. The 3rd process which forms a layer insulation film so that the aforementioned semiconductor device may be embedded. The 4th process which grinds the aforementioned layer insulation film so that the aforementioned layer insulation film may remain on the aforementioned semiconductor device and flattening of the front face of the aforementioned layer insulation film may be carried out, The 5th process which carries out etchback of the whole surface of the aforementioned layer insulation film until a part of cap insulator layer formed on the aforementioned electric conduction film of the best layer among each electric conduction film used as the component of the aforementioned semiconductor device embedded in the aforementioned layer insulation film is exposed first, and carries out flattening of the front face of the aforementioned layer insulation film.

[Claim 6] The manufacture method of a semiconductor device according to claim 5 that the aforementioned semiconductor device is characterized by the bird clapper from the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell.

[Claim 7] The manufacture method of a semiconductor device according to claim 5 or 6 that the aforementioned cap insulator layer formed on the aforementioned electric conduction film of the aforementioned best layer is characterized by the bird clapper from a silicon oxide or a silicon nitride.

[Claim 8] The manufacture method of a semiconductor device given in any 1 term of the claims 5-7 characterized by having further the 6th process which forms the upper insulator layer on the aforementioned layer insulation film after the 5th process of the above.

[Claim 9] The semiconductor device with which it comes to form a semiconductor device on a semiconductor substrate including the element formation field which is equipped with the following, and is characterized by the thing which are located in the topmost part of the 1st insulator layer of the above at least, and which is done for flattening of the aforementioned front face of the 2nd insulator layer of the above in the front face of the 2nd insulator layer of the above while grade is exposed in part, and which was surrounded by isolation structure and demarcated. The 1st insulator layer formed so that the whole surface of the aforementioned semiconductor substrate including the aforementioned semiconductor device top might be worn. The 2nd insulator layer thickly formed as compared with the 1st insulator layer concerned on the insulator layer of the above 1st so that the aforementioned semiconductor device might be embedded.

[Claim 10] The semiconductor device according to claim 9 with which the aforementioned semiconductor device is characterized by the bird clapper from the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell.
[Claim 11] The semiconductor device according to claim 9 or 10 with which the 1st insulator layer of the above is characterized by the bird clapper from a silicon oxide or a silicon nitride.
[Claim 12] In the semiconductor device with which it comes to form a semiconductor device on a semiconductor substrate including the element formation field which was surrounded by isolation structure and demarcated It has the layer insulation film formed so that the aforementioned semiconductor device might be embedded. in the front face of the aforementioned layer insulation film The cap insulator layer formed on the aforementioned electric conduction film of the best layer among each electric conduction film used as the component of the aforementioned semiconductor device is the semiconductor device characterized by carrying out flattening of the aforementioned front face of the aforementioned layer insulation film while grade is exposed a part.
[Claim 13] The semiconductor device according to claim 12 with which the aforementioned semiconductor device is characterized by the bird clapper from the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell.
[Claim 14] The semiconductor device according to claim 12 or 13 with which the aforementioned cap insulator layer formed on the aforementioned electric conduction film of the aforementioned best layer is characterized by the bird clapper from a silicon oxide or a silicon nitride.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention is applied to the semiconductor device with which a remarkable level difference consists in a memory cell and its circumference circuit section like DRAM etc., concerning a semiconductor device and its manufacture method, and is especially suitable.
[0002]
[Description of the Prior Art] In recent years, although horizontal detailed-ization is advancing with high integration of a semiconductor device, it compares with it, and resistance reduction of insulating reservation of a layer insulation film or wiring serves as a technical problem, and vertical thin film-ization has it in the present condition which is not progressing so much. for this reason, a level difference remarkable between the memory cell portion to which the laminating of gate wiring or the insulator layer was carried out with high density, and the circumference circuit portion which controls the memory cell portion concerned if semiconductor memories, such as DRAM, are taken for an example -- being generated -- the upper wiring and contact -- the variation and poor resolving of a size occur at the time of patterning in the photo lithography process of a hole In order to cancel this level difference, layer insulation films, such as a BPSG (Boro-Phospho Silicate Glass) film, are formed all over including a memory cell portion and circumference circuit portion top, a reflow is given, and the method of giving the polish and etchback by the CMP (ChemicalMechanical Polishing) method is shown in the front face.
[0003]
[Problem(s) to be Solved by the Invention] However, flattening by the CMP method is inferior to the polish homogeneity of a layer insulation film, or repeatability between the semiconductor substrates in a semiconductor substrate side, and its variation in the thickness of polish **** is large. for this reason, the variation of the thickness of the layer insulation film which consists in a lower layer in the photo lithography process after flattening -- a reflection factor -- changing -- repeatability -- good -- wiring and contact -- there is a problem that patterning of a hole cannot be performed Moreover, if flattening is not obtained so much at all by the method of giving a reflow to a layer insulation film and carrying out etchback of the front face when a reflow is completed, it is difficult to cancel the global level difference of a memory cell portion and a circumference circuit portion.
[0004] Hereafter, some examples of the flattening method using CMP or etchback are shown below.
[0005] First, the memory cell section and the circumference circuit section are covered, an application film is formed so that flattening of the front face may be carried out, an ion implantation is performed to JP,7-99195,A so that an impurity may reach the upper part of the memory cell section, and the way wet etching (dry etching and polish are sufficient.) removes the impurity pouring layer of the memory cell section with an application film is indicated. According to this method, sufficient flattening of the thing which can make the level difference of the memory cell section and the circumference circuit section a certain grade ease is not obtained, but un-arranging [of an ion-implantation process increasing moreover] is invited
[0006] Next, after forming a silicon oxide in JP,7-297187,A so that wiring may be covered, the method of giving etchback so that may deposit a silicon nitride further, polish removal of the surface may be carried out so that a silicon nitride may remain, a part of silicon oxide may remain after an appropriate time and a silicon nitride may be removed is indicated. Although a certain amount of flattening is obtained, it cannot make a big level difference ease like between the memory cell section and the circumference circuit sections in this method, if thickness like wiring of one layer is thin, since the etch rate of a silicon oxide and a silicon nitride is large with a natural thing and it differs.
[0007] Next, although the method of grinding and carrying out flattening of the front face is indicated after forming a layer insulation film in JP,8-45882,A so that various wiring etc. may be covered, about this method, as mentioned already, it is inferior to polish homogeneity or repeatability, and there is a problem that the variation in the thickness of polish **** is large.
[0008] Next, the method of giving CMP by using as a stopper the silicon nitride formed in order to have filled up the insulator layer for isolation with the insulator layer in the trench (slot) and to form this slot in JP,8-227935,A is indicated. Although according to this method] the void of the insulator layer for isolation is removed and the high semiconductor device of a degree of integration is obtained, application is primarily limited to the isolation structure of a trench type [method / this].
[0009] Then, the purpose of this invention is offering the semiconductor device which can obtain sufficient flattening by simple technique and enables realization of the further high integration, and its manufacture method in the semiconductor device which has a size level difference between the memory cell section and the circumference circuit section like DRAM.
[0010]

[Means for Solving the Problem] The 1st process at which the manufacture method of the semiconductor device of this invention forms isolation structure in the isolation field on a semiconductor substrate, The 2nd process which forms a semiconductor device on the above-mentioned semiconductor substrate including the element formation field which was surrounded by the above-mentioned isolation structure and demarcated, So that the 3rd process which forms the 1st insulator layer so that the whole surface of the aforementioned semiconductor substrate including the aforementioned semiconductor device top may be worn, and the aforementioned semiconductor device may be embedded The 4th process which forms the 2nd thick insulator layer as compared with the 1st insulator layer concerned on the insulator layer of the above 1st, The 5th process which grinds the 2nd insulator layer of the above so that the 2nd insulator layer of the above may remain on the insulator layer of the above 1st and flattening ~~of the front face of the 2nd insulator~~ layer of the above may be carried out, It has the 6th process which carries out etchback of the whole surface of the 2nd insulator layer of the above until a part of 1st insulator layer of the above is exposed first, and carries out flattening of the front face of the 2nd insulator layer of the above.

[0011] The aforementioned semiconductor device consists of the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell in the example of 1 mode of the manufacture method of the semiconductor device of this invention.

[0012] The 1st insulator layer of the above consists of a silicon oxide or a silicon nitride in the example of 1 mode of the manufacture method of the semiconductor device of this invention.

[0013] The example of 1 mode of the manufacture method of the semiconductor device of this invention has further the 7th process which forms the 3rd insulator layer on the insulator layer of the above 2nd after the 6th process of the above.

[0014] The 1st process at which the manufacture method of the semiconductor device of this invention forms isolation structure in the isolation field on a semiconductor substrate, The 2nd process which forms a semiconductor device on the above-mentioned semiconductor substrate including the element formation field which was surrounded by the above-mentioned isolation structure and demarcated, The 3rd process which forms a layer insulation film so that the aforementioned semiconductor device may be embedded, The 4th process which grinds the aforementioned layer insulation film so that the aforementioned layer insulation film may remain on the aforementioned semiconductor device and flattening of the front face of the aforementioned layer insulation film may be carried out, It has the 5th process which carries out etchback of the whole surface of the aforementioned layer insulation film until a part of cap insulator layer formed on the aforementioned electric conduction film of the best layer among each electric conduction film used as the component of the aforementioned semiconductor device embedded in the aforementioned layer insulation film is exposed first, and carries out flattening of the front face of the aforementioned layer insulation film.

[0015] The aforementioned semiconductor device consists of the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell in the example of 1 mode of the manufacture method of the semiconductor device of this invention.

[0016] In the example of 1 mode of the manufacture method of the semiconductor device of this invention, the aforementioned cap insulator layer formed on the aforementioned electric conduction film of the aforementioned best layer consists of a silicon oxide or a silicon nitride.

[0017] The example of 1 mode of the manufacture method of the semiconductor device of this invention has further the 6th process which forms the upper insulator layer on the aforementioned layer insulation film after the 5th process of the above.

[0018] The semiconductor device of this invention is a semiconductor device with which it comes to form a semiconductor device on a semiconductor substrate including the element formation field which was surrounded by isolation structure and demarcated. So that the 1st insulator layer formed so that the whole surface of the aforementioned semiconductor substrate including the aforementioned semiconductor device top might be worn, and the aforementioned semiconductor device may be embedded It has the 2nd insulator layer thickly formed as compared with the 1st insulator layer concerned on the insulator layer of the above 1st, and while one part located in the topmost part of the 1st insulator layer of the above at least is exposed to the front face of the 2nd insulator layer of the above, flattening of the aforementioned front face of the 2nd insulator layer of the above is carried out.

[0019] The aforementioned semiconductor device consists of the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell in the example of 1 mode of the semiconductor device of this invention.

[0020] The 1st insulator layer of the above consists of a silicon oxide or a silicon nitride in the example of 1 mode of the semiconductor device of this invention.

[0021] The semiconductor device of this invention is a semiconductor device with which it comes to form a semiconductor device on a semiconductor substrate including the element formation field which was surrounded by isolation structure and demarcated. It has the layer insulation film formed so that the aforementioned semiconductor device might be embedded. in the front face of the aforementioned layer insulation film While one part of the cap insulator layer formed on the aforementioned electric conduction film of the best layer among each electric conduction film used as the component of the aforementioned semiconductor device is exposed, flattening of the aforementioned front face of the aforementioned layer insulation film is carried out.

[0022] The aforementioned semiconductor device consists of the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell in the example of 1 mode of the semiconductor device of this invention.

[0023] In the example of 1 mode of the semiconductor device of this invention, the aforementioned cap insulator layer formed on the aforementioned electric conduction film of the aforementioned best layer consists of a silicon oxide or a silicon nitride.

[0024]
[Function] It faces manufacturing a semiconductor device and there are a grinding method and the etchback method as the leading technique of the flattening method of the layer insulation film. While the grinding method is excellent in the dissolution of a global level difference, it is inferior to polish homogeneity a little. On the other hand, since it excels in polish homogeneity, and the level difference after deposition of a layer insulation film is reflected while repeatability is good, since a terminal point judging is also easy, the etchback method is unsuitable to the dissolution of a global level difference. this invention uses these two flattening methods together, and it applies only the advantage to the manufacture method of a semiconductor device while it compensates mutual demerit.
[0025] That is, in the manufacture method of the semiconductor device of this invention, the front face of the 2nd insulator layer (layer insulation film) which embeds a semiconductor device is ground first. At this time, flattening of the front face of the 2nd insulator layer (layer insulation film) can fully be carried out, and reduction of a global level difference is made good. However, it is inferior to polish homogeneity, such as a layer insulation film, and repeatability between the semiconductor substrates within a semiconductor substrate side, and dispersion in the amount of polishes (**** of a layer insulation film) is large. Then, etchback of the front face of the 2nd insulator layer (layer insulation film) by which flattening was carried out to some extent is carried out. Since etchback is given by using a part of 1st insulator layer or a part of cap insulator layer as a stopper until a part of cap insulator layer formed on the aforementioned electric conduction film of the best layer among each electric conduction film used as a part of 1st insulator layer of a wrap and the component of a semiconductor device exposes first the semiconductor device embedded at the 2nd insulator layer (layer insulation film) at this time namely, the end time of etchback is specified certainly. Therefore, the 2nd insulator layer (layer insulation film) will have a final very high precision, and will be carried out [flattening] by the etchback following polish.
[0026]
[Embodiments of the Invention] Hereafter, the form of some concrete operations which applied this invention is explained in detail, referring to a drawing.
[0027] (1st operation form) First, the 1st operation form is explained. In this 1st operation form, DRAM is illustrated as a semiconductor device and the composition is explained with the manufacture method. In addition, with the 1st operation form, a memory capacitor explains taking the case of the so-called DRAM of the COB (Capacitor Over Bitline) structure where it is located in the upper layer of bit wiring.
[0028] First, as shown in drawing 1 (a), on the p type silicon semiconductor substrate 1, the field shield isolation structure 22 is formed in an isolation field by the so-called field shield isolation method, and the element formation field 21 is demarcated.
[0029] That is, thickness is first formed for a silicon oxide 2, the polycrystal silicon film 3, and a silicon oxide 4 one by one on the p type silicon semiconductor substrate 1 at 50nm, 200nm, and about 200nm, respectively. Then, patterning of these silicon oxides 2, the polycrystal silicon film 3, and the silicon oxide 4 is carried out by the dry etching following photo lithography and it etc., it removes alternatively, respectively, and the element formation field 21 is demarcated. And after forming a silicon oxide on the whole surface so that the silicon oxide 2, the polycrystal silicon film 3, and silicon oxide 4 which remained may be covered, anisotropy dry etching of the whole surface of the silicon oxide concerned is carried out by RIE etc., it leaves a silicon oxide only to the side attachment wall of a silicon oxide 2, the polycrystal silicon film 3, and a silicon oxide 4, and the side-attachment-wall protective coat 5 is formed. Thereby, the field shield isolation structure 22 equipped with the shield plate electrode which consists of a polycrystal silicon film surrounded by the silicon oxide is formed in a field field.
[0030] Next, as shown in drawing 1 (b), it oxidizes thermally on the front face of the silicon semiconductor substrate 1 on the element formation field 21 which was mutually separated by the field shield isolation structure 22, and was demarcated relatively, and the gate oxide film 6 of about 15nm of thickness is formed. Then, a polycrystal silicon film and a silicon oxide are formed one by one by CVD all over including the field shield isolation structure 22. Subsequently, patterning of these silicon oxides and the polycrystal silicon film is carried out, and the gate electrode 8 which consists of the cap insulator layer 7 and polycrystal silicon film which become band-like from a silicon oxide is formed on the element formation field 21 ranging over the field shield isolation structure 22 top.
[0031] Then, while anisotropy dry etching of the whole surface of the silicon oxide concerned is continuously carried out deposition formation of the silicon oxide and carried out to the whole surface by RIE etc. with CVD so that each cap insulator layer 7 on the element formation field 21 and the field shield isolation structure 22 may be covered, and removing the gate oxide film 6 between the gate electrodes 8 in the element formation field 21, it leaves the above-mentioned silicon oxide only to the side attachment wall of each gate electrode 8, and the side-attachment-wall protective coat 9 is formed. At this time, it has the gate electrode 8 by which pattern formation was carried out to band-like through the gate insulator layer 6 on the element formation field 21 so that the field shield isolation structure 22 top may be straddled, and the gate electrode structure 23 which the cap insulator layer 7 and the side-attachment-wall protective coat 9 are formed, and becomes so that this gate electrode 8 may be covered is completed.
[0032] Next, as shown in drawing 1 (c), deposition formation of the polycrystal silicon film which n type impurity, for example, Lynn (P), is doped by CVD, and becomes is carried out all over including the field shield isolation structure 22 top. At this time, Lynn (P) in the polycrystal silicon film concerned is spread from a polycrystal silicon film on both sides of the gate electrode 8 in the element formation field 21 of the silicon semiconductor substrate 1, and each diffusion layer 10 used as the source/drain is formed.
[0033] Then, patterning of the polycrystal silicon film is carried out to the shape of an island so that it may be divided on the cap

insulator layer 7 on the element formation field 21, and the pad polycrystal silicon film 11 is formed so that it may connect with each diffusion layer 10 independently respectively. Each pad polycrystal silicon film 11 will be formed in the shape of [to which the edge covers the part on the gate electrode structure 23] an island.

[0034] Next, as shown in drawing 2 (a), deposition formation of the layer insulation film 12 which consists of a silicon oxide (SiOX film) by reduced pressure CVD is carried out at about 100nm of thickness. Then, after carrying out deposition formation of the layer insulation film 13 which consists of a BPSG film by ordinary-pressure CVD at about 600nm of thickness so that the layer insulation film 12 may be covered, and giving a reflow, only about 100-200nm only of thickness carries out polish removal of the surface part of the layer insulation film 13 by the chemical machinery grinding (Chemical Mechanical Polishing;CMP) method.

[0035] Next, as shown in drawing 2 (b), whole surface etchback processing is shortly performed to the layer insulation film 13 to which flattening of the front face was carried out to some extent by the CMP method by the dry etching method. Etching gas is made into the mixed gas of CHF3 (60sccm), CF4 (60sccm), and Ar (800sccm), using an parallel monotonous type etching system for example as etching conditions, an etching pressure is set to 1700mTorr(s) and injection power is set to 750W with RF power. Here, if etching of the layer insulation film 13 progresses by etchback processing, the layer insulation film 12 of a wrap part will expose the pad polycrystal silicon film 11 applied on the gate electrode structure 23 where it is located on the field shield isolation structure 22 the topmost part grade of the layer insulation film 12 which consists in the lower layer of the layer insulation film 13 soon, and here. At this time, the etching area of the layer insulation film 13 decreases, and CO emission spectrum intensity in plasma also decreases in connection with it. With this operation form, the variation of this CO emission spectrum intensity is detected, and the time of the layer insulation film 12 being exposed is specified to the terminal point of etching. In addition, even if it ends etching in fact at the time concerned, since the layer insulation film 12 has thin thickness, the topmost part grade of the pad polycrystal silicon film 11 will expose it a little. In this operation form, repeatability can fully improve the whole surface mostly flattening of the layer insulation film 13 in the minimum thickness by the aforementioned etchback processing following the surface polish by the CMP method.

[0036] Next, it is SiOX by reduced pressure CVD on the layer insulation film 13 by which flattening was carried out as shown in drawing 3 (a). Deposition formation of the layer insulation film 14 which consists of a film is carried out at about 100nm of thickness. then, the bit contact in which patterning of the layer insulation films 14, 13, and 12 is carried out, and a part of front face of the pad polycrystal silicon film 11 (pad polycrystal silicon film 11 of the inside of drawing and center-section grade) is exposed -- a hole 15 is formed

[0037] next, it is shown in drawing 3 (b) -- as -- bit contact -- the polycrystal silicon film 16 which doped n type impurity, for example, Lynn, by reduced pressure CVD all over the layer insulation film 14 containing the internal surface of a hole 15 is formed in about 60nm of thickness Then, the tungsten silicide film 17 is formed by the spatter or CVD on the polycrystal silicon film 16 at about 200nm of thickness. And patterning of the tungsten silicide film 17 and the polycrystal silicon film 16 is carried out, and the band-like bit wiring 24 is formed.

[0038] although illustration was omitted after an appropriate time -- a layer insulation film and contact -- pass processes, such as formation of a hole and a memory capacitor, and formation of the metal wiring following it, -- DRAM is completed

[0039] As mentioned above, in the 1st operation form, the front face of the layer insulation film 13 which embeds the gate electrode structure 23 and the pad polycrystal silicon film 11 through the layer insulation film 12 is ground first. At this time, flattening of the front face of the layer insulation film 13 can fully be carried out, and reduction of a global level difference is made good. However, it is inferior to the polish homogeneity of the layer insulation film 13 and repeatability between the silicon semiconductor substrates 1 within the field of the silicon semiconductor substrate 1, and dispersion in the amount of polishes (**** of the layer insulation film 13) is large. Then, etchback of the front face of the layer insulation film 13 by which flattening was carried out to some extent is carried out. Since etchback is given by using some layer insulation films 12 as a stopper until the best layer grade of the layer insulation film 12 formed in the lower layer of the layer insulation film 13 is exposed first at this time namely, the end time of etchback is specified certainly. Therefore, the layer insulation film 13 will have a final very high precision, and will be carried out [flattening] by the etchback following polish.

[0040] Therefore, according to the 1st operation form, in DRAM which has a size level difference between a memory cell field and a circumference circuit field, sufficient flattening can be obtained by simple technique and it becomes realizable [the further high integration].

[0041] - Modification - Here, the modification of the 1st operation form is explained. Although DRAM is manufactured through the almost same process as the 1st operation form in this modification, it is SiOX about the layer insulation film 12. It forms from a silicon nitride (Si3 N4 film) instead of being made from a film.

[0042] Thus, Si 3N4 By forming the layer insulation film 12 which consists of a film, it adds to the effect of the 1st operation form mentioned above, and is Si 3N4. A film is SiOX. As compared with a film, since the etch rate is low, the layer insulation film 12 can function on accuracy as a stopper more at the time of etchback processing, and flattening of the layer insulation film 13 can be performed still more certainly.

[0043] (2nd operation form) Then, the 2nd operation form of this invention is explained. Here, the composition of DRAM is illustrated with the manufacture method like the 1st operation form. Drawing 4 - drawing 9 are the outline cross sections showing the main processes of the manufacture method of DRAM of the 2nd operation form. Drawing where drawing 4 (a) - drawing 4 (c) and drawing 5 (a), drawing 6 (a), drawing 7 (a), drawing 8 (a), and drawing 9 (a) met the longitudinal direction of bit wiring, drawing 5 (b), drawing 6 (b), drawing 7 (b), drawing 8 (b), and drawing 9 (b) are drawings which met in the direction which

intersects perpendicularly with a longitudinal direction. In addition, a same sign is given to the same part as the component of DRAM of the 1st operation form.

[0044] In this 2nd operation form, the field shield layer insulation film 22 and the gate electrode structure 23 are first formed through the process of drawing 1 (a) - drawing 1 (b) like the case of the 1st operation form. Here, the element formation field 21 in which a memory capacitor etc. is formed behind is set to memory cell field 21a, and other element formation fields 21 which adjoin this memory cell are set to circumference circuit field 21b. The gate electrode structure 31 is formed in this circumference circuit field 21b simultaneously with the gate electrode structure 23 in memory cell field 21a.

[0045] Next, as shown in drawing 4 (a), deposition formation of the polycrystal silicon film with which CVD comes to dope n type impurity, for example, Lynn (P), is carried out all over including a memory cell field 21a and circumference circuit field 21b top. At this time, Lynn (P) in the polycrystal silicon film concerned is spread from a polycrystal silicon film on both sides of the gate electrode 8 in memory cell field 21a of the silicon semiconductor substrate 1, and circumference circuit field 21b, and each diffusion layer 33 from which each diffusion layer 10 used as the source/drain serves as the source/drain at circumference circuit field 21b is formed in memory cell field 21a, respectively.

[0046] Then, patterning of the polycrystal silicon film is carried out to the shape of an island so that it may be divided on the cap insulator layer 7 in memory cell field 21a and circumference circuit field 21b, respectively, and the pad polycrystal silicon film 32 is formed in memory cell field 21a, respectively so that it may connect with each diffusion layer 10 independently respectively and the pad polycrystal silicon film 11 may be respectively connected with each diffusion layer 33 independently at circumference circuit field 21b. Each pad polycrystal silicon films 11 and 32 will be formed in the shape of [to which the edge covers the part on the gate electrode structure 23 and 31] an island.

[0047] next, the whole surface which includes a memory cell field 21a and circumference circuit field 21b top as shown in drawing 4 (b) -- CVD -- SiOX the bit contact in which patterning of this layer insulation film 25 is carried out, and a part of front face of the pad polycrystal silicon film 11 (pad polycrystal silicon film 11 of the inside of drawing and the center-section grade in memory cell field 21a) is exposed after forming the layer-insulation film 25 which consists of a film -- a hole 15 is formed

[0048] next, it is shown in drawing 4 (c) -- as -- memory cell field 21a -- setting -- bit contact -- the polycrystal silicon film 16 which doped n type impurity, for example, Lynn, by reduced pressure CVD all over the layer insulation film 25 containing the internal surface of a hole 15 is formed in about 60nm of thickness Then, the tungsten silicide film 17 is formed by the spatter or CVD on the polycrystal silicon film 16, and the silicon nitride (Si3 N4 film) 18 is further formed one by one on the tungsten silicide film 17 at about 200nm of thickness. And Si 3N4 Patterning of a film 18, the tungsten silicide film 17, and the polycrystal silicon film 16 is carried out, and the band-like bit wiring 24 is formed. Here, it is Si 3N4. A film 18 turns into a cap insulator layer of the bit wiring 24.

[0049] Then, it is Si 3N4 by CVD to the whole surface which includes a memory cell field 21a and circumference circuit field 21b top as shown in drawing 5 (a) and drawing 5 (b). A film is formed and it is this Si 3N4. Anisotropic etching of the membranous whole surface is carried out, and the side-attachment-wall protective coat 43 is formed in the side of the bit wiring 24 and the cap insulator layer 18. In addition, drawing 5 (b) shows the cross section of the direction which intersects perpendicularly with the longitudinal direction of the bit wiring 24, and is a cross section corresponding to 1 of dashed line A-A' of drawing 5 (a). This is the same also in the following drawing 6 - drawing 9 .

[0050] Next, as shown in drawing 6 (a) and drawing 6 (b), after carrying out deposition formation of the layer insulation film 44 which consists of a BPSG film by ordinary-pressure CVD all over including a memory cell field 21a and circumference circuit field 21b top at about 4000A of thickness and giving a reflow, only about 100-200nm only of thickness carries out polish removal of the surface part of the layer insulation film 44 by the CMP method.

[0051] Next, as shown in drawing 7 (a) and drawing 7 (b), whole surface etchback processing is shortly performed to the layer insulation film 44 to which flattening of the front face was carried out to some extent by the CMP method by the dry etching method. Etching gas is made into the mixed gas of CHF3 (60sccm), CF4 (60sccm), and Ar (800sccm), using an parallel monotonous type etching system for example as etching conditions, an etching pressure is set to 1700mTorr(s) and injection power is set to 750W with RF power Here, if etching of the layer insulation film 44 progresses by etchback processing, the front face of the cap insulator layer 18 of the bit wiring 24 which consists in the lower layer of the layer insulation film 44 soon will be exposed. At this time, the etching area of the layer insulation film 44 decreases, and CO emission spectrum intensity in plasma also decreases in connection with it. With this operation form, the variation of this CO emission spectrum intensity is detected, and the time of the cap insulator layer 18 being exposed is specified to the terminal point of etching. In this operation form, repeatability can fully improve the whole surface mostly flattening of the layer insulation film 44 in the minimum thickness by the aforementioned etchback processing following the surface polish by the CMP method.

[0052] Next, it is SiOX by reduced pressure CVD to the whole surface so that the bit wiring 24 and the cap insulator layer 18 may be covered, as shown in drawing 8 (a) and drawing 8 (b). Although illustration is omitted after forming in about 200nm of thickness the layer insulation film 34 which consists of a film the storage contact in which patterning of the layer insulation films 34, 44, and 25 is carried out, and a part of front face of the pad polycrystal silicon film 11 (pad polycrystal silicon film 11 of the inside of drawing and the both-ends grade in memory cell field 21a) is exposed -- a hole is formed then, storage contact -- a hole -- the polycrystal silicon film which doped n type impurity, for example, Lynn, by reduced pressure CVD all over including inside is formed in about 460nm of thickness then, a polycrystal silicon film -- patterning -- carrying out -- storage contact -- the storage node electrode 35 which comes to connect with the pad polycrystal silicon film 11 through a hole is formed Then, after forming the dielectric film 36 used as the three-tiered structure of an oxide film, a nitride, and an oxide film so that the storage node

electrode 35 may be covered, the polycrystal silicon film which doped n type impurity, for example, Lynn, by reduced pressure CVD is formed in about 150nm of thickness. Then, patterning of a polycrystal silicon film and the dielectric film 36 is carried out, and the cell plate electrode 37 is formed. At this time, the memory capacitor the storage node electrode 35 and the cell plate electrode 37 counter and carry out [a capacitor] capacity coupling through a dielectric film 36 is completed.

[0053] Next, it is SiOX by CVD to the whole surface which includes a memory cell field 21a and circumference circuit field 21b top so that a memory capacitor may be covered as shown in drawing 9 (a) and drawing 9 (b). After forming a film in about 100nm of thickness, a BPSG film is continuously formed in about 500nm of thickness by ordinary-pressure CVD, and the layer insulation film 38 whose sum total thickness is about 600nm is formed. then, the contact which leads to the gate electrode 8 in circumference circuit field 21b -- a hole (illustration is omitted) is formed

[0054] although illustration was omitted after an appropriate time -- a layer insulation film and connection -- pass processes, such as formation of a hole, and formation of the metal wiring following it, -- DRAM is completed

[0055] As mentioned above, in the 2nd operation form, the front face of the layer insulation film 44 embedding a memory capacitor etc. is ground first. At this time, flattening of the front face of the layer insulation film 44 can fully be carried out, and reduction of a global level difference is made good. However, it is inferior to the polish homogeneity of the layer insulation film 44 and repeatability between the silicon semiconductor substrates 1 within the field of the silicon semiconductor substrate 1, and dispersion in the amount of polishes (**** of the layer insulation film 44) is large. Then, etchback of the front face of the layer insulation film 44 by which flattening was carried out to some extent is carried out. Since etchback is given by using the cap insulator layer 18 as a stopper until the front face of the cap insulator layer 18 located in the lower layer of the layer insulation film 44 is exposed first at this time namely, the end time of etchback is specified certainly. Therefore, from on memory cell field 21a, the layer insulation film 44 will chip on circumference circuit field 21b, and will be carried out [flattening] with a final very high precision by the etchback following polish.

[0056] Therefore, according to the 2nd operation form, in DRAM which has a size level difference between memory cell field 21a and circumference circuit field 21b, sufficient flattening can be obtained by simple technique and it becomes realizable [the further high integration].

[0057] (3rd operation form) Then, the 3rd operation form of this invention is explained. Here, an MOS transistor is illustrated as a semiconductor device and the composition is explained with the manufacture method. In addition, a same sign is given to the same part as the component of DRAM of the 1st operation form.

[0058] First, like the case of the 1st operation form, through the process of drawing 1 (a), the field shield layer insulation film 22 is formed, and the element formation field 21 is demarcated on the silicon semiconductor substrate 1 in this 3rd operation form.

[0059] Next, as shown in drawing 10 (a), it oxidizes thermally on the front face of the silicon semiconductor substrate 1 on the element formation field 21, and the gate oxide film 6 of about 110nm of thickness is formed. Then, they are a polycrystal silicon film and Si 3N4 by CVD to the whole surface including the field shield isolation structure 22. A film is formed one by one so that thickness may be set to about 200-300nm and about 20-50nm, respectively. Subsequently, these Si 3N4 Patterning of a film and the polycrystal silicon film is carried out, the field shield isolation structure 22 top is straddled, and it is Si 3N4 to band-like on the element formation field 21. The gate electrode 8 which consists of the cap insulator layer 51 and polycrystal silicon film which consist of a film is formed.

[0060] Then, a silicon oxide is formed in the whole surface by CVD, anisotropic etching of the whole surface of this silicon oxide is carried out, the side-attachment-wall protective coat 52 is formed in the side of each gate electrode 8 and the cap insulator layer 51, and the gate electrode structure 53 is formed.

[0061] Next, after forming the BPSG film 54 in about 600nm by ordinary-pressure CVD here [the thickness and here] where the gate electrode structure 53 on the element formation field 21 is embedded after forming a silicon oxide 55 in about 100nm of thickness so that the whole surface may be worn by CVD as shown in drawing 10 (b), and giving a reflow, only about 100-200nm only of thickness carries out polish removal of the surface part of the layer insulation film 54 by the CMP method.

[0062] Next, as shown in drawing 10 (c), whole surface etchback processing is shortly performed to the layer insulation film 54 to which flattening of the front face was carried out to some extent by the CMP method by the dry etching method. Etching gas is made into the mixed gas of CHF3 (60sccm), CF4 (60sccm), and Ar (800sccm), using an parallel monotonous type etching system for example as etching conditions, an etching pressure is set to 1700mTorr(s) and injection power is set to 750W with RF power. Here, if etching of the layer insulation film 54 progresses by etchback processing, the front face of the cap insulator layer 51 of the gate electrode structure 53 which consists soon on the lower layer field shield isolation structure 22 of the layer insulation film 54 will be exposed. At this time, the etching area of the layer insulation film 54 decreases, and CO emission spectrum intensity in plasma also decreases in connection with it. With this operation form, the variation of this CO emission spectrum intensity is detected, and the time of the cap insulator layer 52 being exposed is specified to the terminal point of etching. In this operation form, repeatability can fully improve the whole surface mostly flattening of the layer insulation film 54 in the minimum thickness by the aforementioned etchback processing following the surface polish by the CMP method.

[0063] although illustration was omitted after an appropriate time -- a memory cell capacitor, a layer insulation film, and connection -- pass processes, such as formation of a hole, and formation of the metal wiring following it, -- an MOS transistor is completed

[0064] As mentioned above, in the 3rd operation gestalt, the front face of the layer insulation film 54 which embeds the gate electrode structure 53 is ground first. Etchback of the front face of the layer insulation film 54 at this time by which flattening was carried out to some extent is carried out. At this time, flattening of the front face of the layer insulation film 54 can fully be carried

out, and reduction of a global level difference is made good. However, it is inferior to the polish homogeneity of the layer insulation film 54 and repeatability between the silicon semiconductor substrates 1 within the field of the silicon semiconductor substrate 1, and dispersion in the amount of polishes (**** of the layer insulation film 54) is large. Since etchback is given by using the cap insulator layer 51 as a stopper until the front face of the cap insulator layer 51 located in the lower layer of the layer insulation film 54 is exposed first namely, the end time of etchback is specified certainly. Therefore, the layer insulation film 54 will have a final very high precision, and will be carried out [flattening] by the etchback following polish.

[0065] in addition, the 1- above-mentioned [this invention] -- it is not limited to the 3rd operation ****** For example, instead of forming isolation structure as field shield isolation structure by the field shield isolation method, it forms as a field oxide film by the so-called LOCOS method, or a slot is formed in a silicon semiconductor substrate by the trench separation method, this Mizouchi may be embedded by the insulator layer and trench type isolation structure may be formed.

[0066]

[Effect of the Invention] According to this invention, in DRAM, an MOS transistor with a big level difference, etc. which have a size level difference, for example between a memory cell field and a circumference circuit field, sufficient flattening can be obtained by simple technique and it becomes realizable [the further high integration].

[Translation done.]

* NOTICES *

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

TECHNICAL FIELD

[The technical field to which invention belongs] this invention is applied to the semiconductor device with which a remarkable level difference consists in a memory cell and its circumference circuit section like DRAM etc., concerning a semiconductor device and its manufacture method, and is especially suitable.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] In recent years, although horizontal detailed-ization is advancing with high integration of a semiconductor device, it compares with it, and resistance reduction of insulating reservation of a layer insulation film or wiring serves as a technical problem, and vertical thin film-ization has it in the present condition which is not progressing so much. for this reason, a level difference remarkable between the memory cell portion to which the laminating of gate wiring or the insulator layer was carried out with high density, and the circumference circuit portion which controls the memory cell portion concerned if semiconductor memories, such as DRAM, are taken for an example -- being generated -- the upper wiring and contact -- the variation and poor resolving of a size occur at the time of patterning in the photo lithography process of a hole In order to cancel this level difference, layer insulation films, such as a BPSG (Boro-Phospho Silicate Glass) film, are formed all over including a memory cell portion and circumference circuit portion top, a reflow is given, and the method of giving the polish and etchback by the CMP (ChemicalMechanical Polishing) method is shown in the front face.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, in DRAM, an MOS transistor with a big level difference, etc. which have a size level difference, for example between a memory cell field and a circumference circuit field, sufficient flattening can be obtained by simple technique and it becomes realizable [the further high integration].

[Translation done.]

* NOTICES *

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, flattening by the CMP method is inferior to the polish homogeneity of a layer insulation film, or repeatability between the semiconductor substrates in a semiconductor substrate side, and its variation in the thickness of polish **** is large. for this reason, the variation of the thickness of the layer insulation film which consists in a lower layer in the photo lithography process after flattening -- a reflection factor -- changing -- repeatability -- good -- wiring and contact -- there is a problem that patterning of a hole cannot be performed Moreover, if flattening is not obtained so much at all by the method of giving a reflow to a layer insulation film and carrying out etchback of the front face when a reflow is completed, it is difficult to cancel the global level difference of a memory cell portion and a circumference circuit portion.

[0004] Hereafter, some examples of the flattening method using CMP or etchback are shown below.

[0005] First, the memory cell section and the circumference circuit section are covered, an application film is formed so that flattening of the front face may be carried out, an ion implantation is performed to JP,7-99195,A so that an impurity may reach the upper part of the memory cell section, and the way wet etching (dry etching and polish are sufficient.) removes the impurity pouring layer of the memory cell section with an application film is indicated. According to this method, sufficient flattening of the thing which can make the level difference of the memory cell section and the circumference circuit section a certain grade ease is not obtained, but un-arranging [of an ion-implantation process increasing moreover] is invited.

[0006] Next, after forming a silicon oxide in JP,7-297187,A so that wiring may be covered, the method of giving etchback so that may deposit a silicon nitride further, polish removal of the surface may be carried out so that a silicon nitride may remain, a part of silicon oxide may remain after an appropriate time and a silicon nitride may be removed is indicated. Although a certain amount of flattening is obtained, it cannot make a big level difference ease like between the memory cell section and the circumference circuit sections in this method, if thickness like wiring of one layer is thin, since the etch rate of a silicon oxide and a silicon nitride is large with a natural thing and it differs.

[0007] Next, although the method of grinding and carrying out flattening of the front face is indicated after forming a layer insulation film in JP,8-45882,A so that various wiring etc may be covered, about this method, as mentioned already, it is inferior to polish homogeneity or repeatability, and there is a problem that the variation in the thickness of polish **** is large.

[0008] Next, the method of giving CMP by using as a stopper the silicon nitride formed in order to have filled up the insulator layer for isolation with the insulator layer in the trench (slot) and to form this slot in JP,8-227935,A is indicated. Although according to this method] the void of the insulator layer for isolation is removed and the high semiconductor device of a degree of integration is obtained, application is primarily limited to the isolation structure of a trench type [method / this].

[0009] Then, the purpose of this invention is offering the semiconductor device which can obtain sufficient flattening by simple technique and enables realization of the further high integration, and its manufacture method in the semiconductor device which has a size level difference between the memory cell section and the circumference circuit section like DRAM.

[Translation done.]

* NOTICES *

MEANS

[Means for Solving the Problem] It is characterized by equipping the manufacture method of the semiconductor device of this invention with the following. The 1st process which forms isolation structure in the isolation field on a semiconductor substrate. The 2nd process which forms a semiconductor device on the above-mentioned semiconductor substrate including the element formation field which was surrounded by the above-mentioned isolation structure and demarcated. The 3rd process which forms the 1st insulator layer so that the whole surface of the aforementioned semiconductor substrate including the aforementioned semiconductor device top may be worn. The 4th process which forms the 2nd thick insulator layer as compared with the 1st insulator layer concerned on the insulator layer of the above 1st so that the aforementioned semiconductor device may be embedded, The 5th process which grinds the 2nd insulator layer of the above so that the 2nd insulator layer of the above may remain on the insulator layer of the above 1st and flattening of the front face of the 2nd insulator layer of the above may be carried out, The 6th process which carries out etchback of the whole surface of the 2nd insulator layer of the above until a part of 1st insulator layer of the above is exposed first, and carries out flattening of the front face of the 2nd insulator layer of the above.
[0011] The aforementioned semiconductor device consists of the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell in the example of 1 mode of the manufacture method of the semiconductor device of this invention
[0012] The 1st insulator layer of the above consists of a silicon oxide or a silicon nitride in the example of 1 mode of the manufacture method of the semiconductor device of this invention.
[0013] The example of 1 mode of the manufacture method of the semiconductor device of this invention has further the 7th process which forms the 3rd insulator layer on the insulator layer of the above 2nd after the 6th process of the above.
[0014] It is characterized by equipping the manufacture method of the semiconductor device of this invention with the following. The 1st process which forms isolation structure in the isolation field on a semiconductor substrate. The 2nd process which forms a semiconductor device on the above-mentioned semiconductor substrate including the element formation field which was surrounded by the above-mentioned isolation structure and demarcated. The 3rd process which forms a layer insulation film so that the aforementioned semiconductor device may be embedded. The 4th process which grinds the aforementioned layer insulation film so that the aforementioned layer insulation film may remain on the aforementioned semiconductor device and flattening of the front face of the aforementioned layer insulation film may be carried out, The 5th process which carries out etchback of the whole surface of the aforementioned layer insulation film until a part of cap insulator layer formed on the aforementioned electric conduction film of the best layer among each electric conduction film used as the component of the aforementioned semiconductor device embedded in the aforementioned layer insulation film is exposed first, and carries out flattening of the front face of the aforementioned layer insulation film.
[0015] The aforementioned semiconductor device consists of the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell in the example of 1 mode of the manufacture method of the semiconductor device of this invention.
[0016] In the example of 1 mode of the manufacture method of the semiconductor device of this invention, the aforementioned cap insulator layer formed on the aforementioned electric conduction film of the aforementioned best layer consists of a silicon oxide or a silicon nitride.
[0017] The example of 1 mode of the manufacture method of the semiconductor device of this invention has further the 6th process which forms the upper insulator layer on the aforementioned layer insulation film after the 5th process of the above.
[0018] The semiconductor device of this invention is a semiconductor device with which it comes to form a semiconductor device on a semiconductor substrate including the element formation field which was surrounded by isolation structure and demarcated. So that the 1st insulator layer formed so that the whole surface of the aforementioned semiconductor substrate including the aforementioned semiconductor device top might be worn, and the aforementioned semiconductor device may be embedded It has the 2nd insulator layer thickly formed as compared with the 1st insulator layer concerned on the insulator layer of the above 1st, and while one part located in the topmost part of the 1st insulator layer of the above at least is exposed to the front face of the 2nd insulator layer of the above, flattening of the aforementioned front face of the 2nd insulator layer of the above is carried out.
[0019] The aforementioned semiconductor device consists of the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell in the example of 1 mode of the semiconductor device of this invention.
[0020] The 1st insulator layer of the above consists of a silicon oxide or a silicon nitride in the example of 1 mode of the

semiconductor device of this invention.

[0021] The semiconductor device of this invention is a semiconductor device with which it comes to form a semiconductor device on a semiconductor substrate including the element formation field which was surrounded by isolation structure and demarcated. It has the layer insulation film formed so that the aforementioned semiconductor device might be embedded. in the front face of the aforementioned layer insulation film While one part of the cap insulator layer formed on the aforementioned electric conduction film of the best layer among each electric conduction film used as the component of the aforementioned semiconductor device is exposed, flattening of the aforementioned front face of the aforementioned layer insulation film is carried out.

[0022] The aforementioned semiconductor device consists of the 1st element which constitutes a memory cell, and the 2nd element which constitutes the circumference circuit section of the aforementioned memory cell in the example of 1 mode of the semiconductor device of this invention.

[0023] In the example of 1 mode of the semiconductor device of this invention, the aforementioned cap insulator layer formed on the aforementioned electric conduction film of the aforementioned best layer consists of a silicon oxide or a silicon nitride.

[Translation done.]

OPERATION

[Function] It faces manufacturing a semiconductor device and there are a grinding method and the etchback method as the leading technique of the flattening method of the layer insulation film. While the grinding method is excellent in the dissolution of a global level difference, it is inferior to polish homogeneity a little. On the other hand, since it excels in polish homogeneity, and the level difference after deposition of a layer insulation film is reflected while repeatability is good, since a terminal point judging is also easy, the etchback method is unsuitable to the dissolution of a global level difference. this invention uses these two flattening methods together, and it applies only the advantage to the manufacture method of a semiconductor device while it compensates mutual demerit.

[0025] That is, in the manufacture method of the semiconductor device of this invention, the front face of the 2nd insulator layer (layer insulation film) which embeds a semiconductor device is ground first. At this time, flattening of the front face of the 2nd insulator layer (layer insulation film) can fully be carried out, and reduction of a global level difference is made good However, it is inferior to polish homogeneity, such as a layer insulation film, and repeatability between the semiconductor substrates within a semiconductor substrate side, and dispersion in the amount of polishes (**** of a layer insulation film) is large. Then, etchback of the front face of the 2nd insulator layer (layer insulation film) by which flattening was carried out to some extent is carried out. Since etchback is given by using a part of 1st insulator layer or a part of cap insulator layer as a stopper until a part of cap insulator layer formed on the aforementioned electric conduction film of the best layer among each electric conduction film used as a part of 1st insulator layer of a wrap and the component of a semiconductor device exposes first the semiconductor device embedded at the 2nd insulator layer (layer insulation film) at this time namely, the end time of etchback is specified certainly. Therefore, the 2nd insulator layer (layer insulation film) will have a final very high precision, and will be carried out [flattening] by the etchback following polish.

[0026]

[Embodiments of the Invention] Hereafter, the gestalt of some concrete operations which applied this invention is explained in detail, referring to a drawing.

[0027] (1st operation gestalt) First, the 1st operation gestalt is explained. In this 1st operation gestalt, DRAM is illustrated as a semiconductor device and the composition is explained with the manufacture method. In addition, with the 1st operation gestalt, a memory capacitor explains taking the case of the so-called DRAM of the COB (Capacitor Over Bitline) structure where it is located in the upper layer of bit wiring.

[0028] First, as shown in drawing 1 (a), on the p type silicon semiconductor substrate 1, the field shield isolation structure 22 is formed in an isolation field by the so-called field shield isolation method, and the element formation field 21 is demarcated.

[0029] That is, thickness is first formed for a silicon oxide 2, the polycrystal silicon film 3, and a silicon oxide 4 one by one on the p type silicon semiconductor substrate 1 at 50nm, 200nm, and about 200nm, respectively. Then, patterning of these silicon oxides 2, the polycrystal silicon film 3, and the silicon oxide 4 is carried out by the dry etching following photo lithography and it etc., it removes alternatively, respectively, and the element formation field 21 is demarcated. And after forming a silicon oxide on the whole surface so that the silicon oxide 2, the polycrystal silicon film 3, and silicon oxide 4 which remained may be covered, anisotropy dry etching of the whole surface of the silicon oxide concerned is carried out by RIE etc., it leaves a silicon oxide only to the side attachment wall of a silicon oxide 2, the polycrystal silicon film 3, and a silicon oxide 4, and the side-attachment-wall protective coat 5 is formed. Thereby, the field shield isolation structure 22 equipped with the shield plate electrode which consists of a polycrystal silicon film surrounded by the silicon oxide is formed in a field field.

[0030] Next, as shown in drawing 1 (b), it oxidizes thermally on the front face of the silicon semiconductor substrate 1 on the element formation field 21 which was mutually separated by the field shield isolation structure 22, and was demarcated relatively, and the gate oxide film 6 of about 15nm of thickness is formed. Then, a polycrystal silicon film and a silicon oxide are formed one by one by CVD all over including the field shield isolation structure 22. Subsequently, patterning of these silicon oxides and the polycrystal silicon film is carried out, and the gate electrode 8 which consists of the cap insulator layer 7 and polycrystal silicon film which become band-like from a silicon oxide is formed on the element formation field 21 ranging over the field shield isolation structure 22 top.

[0031] Then, while anisotropy dry etching of the whole surface of the silicon oxide concerned is continuously carried out deposition formation of the silicon oxide and carried out to the whole surface by RIE etc. with CVD so that each cap insulator layer 7 on the element formation field 21 and the field shield isolation structure 22 may be covered, and removing the gate oxide film 6 between the gate electrodes 8 in the element formation field 21, it leaves the above-mentioned silicon oxide only to the side

attachment wall of each gate electrode 8, and the side-attachment-wall protective coat 9 is formed. At this time, it has the gate electrode 8 by which pattern formation was carried out to band-like through the gate insulator layer 6 on the element formation field 21 so that the field shield isolation structure 22 top may be straddled, and the gate electrode structure 23 which the cap insulator layer 7 and the side-attachment-wall protective coat 9 are formed, and becomes so that this gate electrode 8 may be covered is completed.

[0032] Next, as shown in drawing 1 (c), deposition formation of the polycrystal silicon film which n type impurity, for example, Lynn (P), is doped by CVD, and becomes is carried out all over including the field shield isolation structure 22 top. At this time, Lynn (P) in the polycrystal silicon film concerned is spread from a polycrystal silicon film on both sides of the gate electrode 8 in the element formation field 21 of the silicon semiconductor substrate 1, and each diffusion layer 10 used as the source/drain is formed.

[0033] Then, patterning of the polycrystal silicon film is carried out to the shape of an island so that it may be divided on the cap insulator layer 7 on the element formation field 21, and the pad polycrystal silicon film 11 is formed so that it may connect with each diffusion layer 10 independently respectively. Each pad polycrystal silicon film 11 will be formed in the shape of [to which the edge covers the part on the gate electrode structure 23] an island.

[0034] Next, as shown in drawing 2 (a), deposition formation of the layer insulation film 12 which consists of a silicon oxide (SiOX film) by reduced pressure CVD is carried out at about 100nm of thickness. Then, after carrying out deposition formation of the layer insulation film 13 which consists of a BPSG film by ordinary-pressure CVD at about 600nm of thickness so that the layer insulation film 12 may be covered, and giving a reflow, only about 100-200nm only of thickness carries out polish removal of the surface part of the layer insulation film 13 by the chemical machinery grinding (Chemical Mechanical Polishing;CMP) method.

[0035] Next, as shown in drawing 2 (b), whole surface etchback processing is shortly performed to the layer insulation film 13 to which flattening of the front face was carried out to some extent by the CMP method by the dry etching method. Etching gas is made into the mixed gas of CHF3 (60sccm), CF4 (60sccm), and Ar (800sccm), using an parallel monotonous type etching system for example as etching conditions, an etching pressure is set to 1700mTorr(s) and injection power is set to 750W with RF power. Here, if etching of the layer insulation film 13 progresses by etchback processing, the layer insulation film 12 of a wrap part will expose the pad polycrystal silicon film 11 applied on the gate electrode structure 23 where it is located on the field shield isolation structure 22 the topmost part grade of the layer insulation film 12 which consists in the lower layer of the layer insulation film 13 soon, and here. At this time, the etching area of the layer insulation film 13 decreases, and CO emission spectrum intensity in plasma also decreases in connection with it. With this operation gestalt, the variation of this CO emission spectrum intensity is detected, and the time of the layer insulation film 12 being exposed is specified to the terminal point of etching. In addition, even if it ends etching in fact at the time concerned, since the layer insulation film 12 has thin thickness, the topmost part grade of the pad polycrystal silicon film 11 will expose it a little. In this operation gestalt, repeatability can fully improve the whole surface mostly flattening of the layer insulation film 13 in the minimum thickness by the aforementioned etchback processing following the surface polish by the CMP method.

[0036] Next, it is SiOX by reduced pressure CVD on the layer insulation film 13 by which flattening was carried out as shown in drawing 3 (a). Deposition formation of the layer insulation film 14 which consists of a film is carried out at about 100nm of thickness. then, the bit contact in which patterning of the layer insulation films 14, 13, and 12 is carried out, and a part of front face of the pad polycrystal silicon film 11 (pad polycrystal silicon film 11 of the inside of drawing and center-section grade) is exposed -- a hole 15 is formed

[0037] next, it is shown in drawing 3 (b) -- as -- bit contact -- the polycrystal silicon film 16 which doped n type impurity, for example, Lynn, by reduced pressure CVD all over the layer insulation film 14 containing the internal surface of a hole 15 is formed in about 60nm of thickness Then, the tungsten silicide film 17 is formed by the spatter or CVD on the polycrystal silicon film 16 at about 200nm of thickness. And patterning of the tungsten silicide film 17 and the polycrystal silicon film 16 is carried out, and the band-like bit wiring 24 is formed.

[0038] although illustration was omitted after an appropriate time -- a layer insulation film and contact -- pass processes, such as formation of a hole and a memory capacitor, and formation of the metal wiring following it, -- DRAM is completed

[0039] As mentioned above, in the 1st operation gestalt, the front face of the layer insulation film 13 which embeds the gate electrode structure 23 and the pad polycrystal silicon film 11 through the layer insulation film 12 is ground first. At this time, flattening of the front face of the layer insulation film 13 can fully be carried out, and reduction of a global level difference is made good. However, it is inferior to the polish homogeneity of the layer insulation film 13 and repeatability between the silicon semiconductor substrates 1 within the field of the silicon semiconductor substrate 1, and dispersion in the amount of polishes (**** of the layer insulation film 13) is large. Then, etchback of the front face of the layer insulation film 13 by which flattening was carried out to some extent is carried out. Since etchback is given by using some layer insulation films 12 as a stopper until the best layer grade of the layer insulation film 12 formed in the lower layer of the layer insulation film 13 is exposed first at this time namely, the end time of etchback is specified certainly. Therefore, the layer insulation film 13 will have a final very high precision, and will be carried out [flattening] by the etchback following polish.

[0040] Therefore, according to the 1st operation gestalt, in DRAM which has a size level difference between a memory cell field and a circumference circuit field, sufficient flattening can be obtained by simple technique and it becomes realizable [the further high integration].

[0041] - Modification - Here, the modification of the 1st operation gestalt is explained. Although DRAM is manufactured through

the almost same process as the 1st operation gestalt in this modification, it is SiOX about the layer insulation film 12. It forms from a silicon nitride (Si3 N4 film) instead of being made from a film.

[0042] Thus, Si 3N4 By forming the layer insulation film 12 which consists of a film, it adds to the effect of the 1st operation gestalt mentioned above, and is Si 3N4. A film is SiOX. As compared with a film, for a low reason, the layer insulation film 12 can function on accuracy as a stopper more at the time of etchback processing, and an etch rate can perform flattening of the layer insulation film 13 still more certainly.

[0043] (2nd operation gestalt) Then, the 2nd operation gestalt of this invention is explained. Here, the composition of DRAM is illustrated with the manufacture method like the 1st operation gestalt. Drawing 4 - drawing 9 are the outline cross sections showing the main processes of the manufacture method of DRAM of the 2nd operation gestalt. Drawing where drawing 4 (a) - drawing 4 (c) and drawing 5 (a), drawing 6 (a), drawing 7 (a), drawing 8 (a), and drawing 9 (a) met the longitudinal direction of bit wiring, drawing 5 (b), drawing 6 (b), drawing 7 (b), drawing 8 (b), and drawing 9 (b) are drawings which met in the direction which intersects perpendicularly with a longitudinal direction. In addition, a same sign is given to the same part as the component of DRAM of the 1st operation gestalt.

[0044] In this 2nd operation gestalt, the field shield layer insulation film 22 and the gate electrode structure 23 are first formed through the process of drawing 1 (a) - drawing 1 (b) like the case of the 1st operation gestalt. Here, the element formation field 21 in which a memory capacitor etc. is formed behind is set to memory cell field 21a, and other element formation fields 21 which adjoin this memory cell are set to circumference circuit field 21b. The gate electrode structure 31 is formed in this circumference circuit field 21b simultaneously with the gate electrode structure 23 in memory cell field 21a.

[0045] Next, as shown in drawing 4 (a), deposition formation of the polycrystal silicon film with which CVD comes to dope n type impurity, for example, Lynn (P), is carried out all over including a memory cell field 21a and circumference circuit field 21b top. At this time, Lynn (P) in the polycrystal silicon film concerned is spread from a polycrystal silicon film on both sides of the gate electrode 8 in memory cell field 21a of the silicon semiconductor substrate 1, and circumference circuit field 21b, and each diffusion layer 33 from which each diffusion layer 10 used as the source/drain serves as the source/drain at circumference circuit field 21b is formed in memory cell field 21a, respectively.

[0046] Then, patterning of the polycrystal silicon film is carried out to the shape of an island so that it may be divided on the cap insulator layer 7 in memory cell field 21a and circumference circuit field 21b, respectively, and the pad polycrystal silicon film 32 is formed in memory cell field 21a, respectively so that it may connect with each diffusion layer 10 independently respectively and the pad polycrystal silicon film 11 may be respectively connected with each diffusion layer 33 independently at circumference circuit field 21b. Each pad polycrystal silicon films 11 and 32 will be formed in the shape of [to which the edge covers the part on the gate electrode structure 23 and 31] an island.

[0047] next, the whole surface which includes a memory cell field 21a and circumference circuit field 21b top as shown in drawing 4 (b) -- CVD -- SiOX the bit contact in which patterning of this layer insulation film 25 is carried out, and a part of front face of the pad polycrystal silicon film 11 (pad polycrystal silicon film 11 of the inside of drawing and the center-section grade in memory cell field 21a) is exposed after forming the layer-insulation film 25 which consists of a film -- a hole 15 is formed

[0048] next, it is shown in drawing 4 (c) -- as -- memory cell field 21a -- setting -- bit contact -- the polycrystal silicon film 16 which doped n type impurity, for example, Lynn, by reduced pressure CVD all over the layer insulation film 25 containing the internal surface of a hole 15 is formed in about 60nm of thickness Then, the tungsten silicide film 17 is formed by the spatter or CVD on the polycrystal silicon film 16, and the silicon nitride (Si3 N4 film) 18 is further formed one by one on the tungsten silicide film 17 at about 200nm of thickness. And Si 3N4 Patterning of a film 18, the tungsten silicide film 17, and the polycrystal silicon film 16 is carried out, and the band-like bit wiring 24 is formed. Here, it is Si 3N4. A film 18 turns into a cap insulator layer of the bit wiring 24.

[0049] Then, it is Si 3N4 by CVD to the whole surface which includes a memory cell field 21a and circumference circuit field 21b top as shown in drawing 5 (a) and drawing 5 (b). A film is formed and it is this Si 3N4. Anisotropic etching of the membranous whole surface is carried out, and the side-attachment-wall protective coat 43 is formed in the side of the bit wiring 24 and the cap insulator layer 18. In addition, drawing 5 (b) shows the cross section of the direction which intersects perpendicularly with the longitudinal direction of the bit wiring 24, and is a cross section corresponding to 1 of dashed line A-A' of drawing 5 (a). This is the same also in the following drawing 6 - drawing 9 .

[0050] Next, as shown in drawing 6 (a) and drawing 6 (b), after carrying out deposition formation of the layer insulation film 44 which consists of a BPSG film by ordinary-pressure CVD all over including a memory cell field 21a and circumference circuit field 21b top at about 4000A of thickness and giving a reflow, only about 100-200nm only of thickness carries out polish removal of the surface part of the layer insulation film 44 by the CMP method.

[0051] Next, as shown in drawing 7 (a) and drawing 7 (b), whole surface etchback processing is shortly performed to the layer insulation film 44 to which flattening of the front face was carried out to some extent by the CMP method by the dry etching method. Etching gas is made into the mixed gas of CHF3 (60sccm), CF4 (60sccm), and Ar (800sccm), using an parallel monotonous type etching system for example as etching conditions, an etching pressure is set to 1700mTorr(s) and injection power is set to 750W with RF power. Here, if etching of the layer insulation film 44 progresses by etchback processing, the front face of the cap insulator layer 18 of the bit wiring 24 which consists in the lower layer of the layer insulation film 44 soon will be exposed. At this time, the etching area of the layer insulation film 44 decreases, and CO emission spectrum intensity in plasma also decreases in connection with it. With this operation gestalt, the variation of this CO emission spectrum intensity is detected, and the time of the cap insulator layer 18 being exposed is specified to the terminal point of etching. In this operation gestalt,

repeatability can fully improve the whole surface mostly flattening of the layer insulation film 44 in the minimum thickness by the aforementioned etchback processing following the surface polish by the CMP method.

[0052] Next, it is SiOX by reduced pressure CVD to the whole surface so that the bit wiring 24 and the cap insulator layer 18 may be covered, as shown in drawing 8 (a) and drawing 8 (b). Although illustration is omitted after forming in about 200nm of thickness the layer insulation film 34 which consists of a film the storage contact in which patterning of the layer insulation films 34. 44, and 25 is carried out, and a part of front face of the pad polycrystal silicon film 11 (pad polycrystal silicon film 11 of the inside of drawing and the both-ends grade in memory cell field 21a) is exposed -- a hole is formed then, storage contact -- a hole -- the polycrystal silicon film which doped n type impurity, for example, Lynn, by reduced pressure CVD all over including inside is formed in about 460nm of thickness then, a polycrystal silicon film -- patterning -- carrying out -- storage contact -- the storage node electrode 35 which comes to connect with the pad polycrystal silicon film 11 through a hole is formed Then, after forming the dielectric film 36 used as the three-tiered structure of an oxide film, a nitride, and an oxide film so that the storage node electrode 35 may be covered, the polycrystal silicon film which doped n type impurity, for example, Lynn, by reduced pressure CVD is formed in about 150nm of thickness. Then, patterning of a polycrystal silicon film and the dielectric film 36 is carried out, and the cell plate electrode 37 is formed. At this time, the memory capacitor the storage node electrode 35 and the cell plate electrode 37 counter and carry out [a capacitor] capacity coupling through a dielectric film 36 is completed.

[0053] Next, it is SiOX by CVD to the whole surface which includes a memory cell field 21a and circumference circuit field 21b top so that a memory capacitor may be covered as shown in drawing 9 (a) and drawing 9 (b). After forming a film in about 100nm of thickness, a BPSG film is continuously formed in about 500nm of thickness by ordinary-pressure CVD, and the layer insulation film 38 whose sum total thickness is about 600nm is formed. then, the contact which leads to the gate electrode 8 in circumference circuit field 21b -- a hole (illustration is omitted) is formed

[0054] although illustration was omitted after an appropriate time -- a layer insulation film and connection -- pass processes, such as formation of a hole, and formation of the metal wiring following it, -- DRAM is completed

[0055] As mentioned above, in the 2nd operation gestalt, the front face of the layer insulation film 44 embedding a memory capacitor etc. is ground first. At this time, flattening of the front face of the layer insulation film 44 can fully be carried out, and reduction of a global level difference is made good. However, it is inferior to the polish homogeneity of the layer insulation film 44 and repeatability between the silicon semiconductor substrates 1 within the field of the silicon semiconductor substrate 1, and dispersion in the amount of polishes (**** of the layer insulation film 44) is large. Then, etchback of the front face of the layer insulation film 44 by which flattening was carried out to some extent is carried out. Since etchback is given by using the cap insulator layer 18 as a stopper until the front face of the cap insulator layer 18 located in the lower layer of the layer insulation film 44 is exposed first at this time namely, the end time of etchback is specified certainly. Therefore, from on memory cell field 21a, the layer insulation film 44 will chip on circumference circuit field 21b, and will be carried out [flattening] with a final very high precision by the etchback following polish.

[0056] Therefore, according to the 2nd operation gestalt, in DRAM which has a size level difference between memory cell field 21a and circumference circuit field 21b, sufficient flattening can be obtained by simple technique and it becomes realizable [the further high integration].

[0057] (3rd operation gestalt) Then, the 3rd operation gestalt of this invention is explained. Here, an MOS transistor is illustrated as a semiconductor device and the composition is explained with the manufacture method. In addition, a same sign is given to the same part as the component of DRAM of the 1st operation gestalt.

[0058] First, like the case of the 1st operation gestalt, through the process of drawing 1 (a), the field shield layer insulation film 22 is formed, and the element formation field 21 is demarcated on the silicon semiconductor substrate 1 in this 3rd operation gestalt.

[0059] Next, as shown in drawing 10 (a), it oxidizes thermally on the front face of the silicon semiconductor substrate 1 on the element formation field 21, and the gate oxide film 6 of about 110nm of thickness is formed. Then, they are a polycrystal silicon film and Si 3N4 by CVD to the whole surface including the field shield isolation structure 22. A film is formed one by one so that thickness may be set to about 200-300nm and about 20-50nm, respectively. Subsequently, these Si 3N4 Patterning of a film and the polycrystal silicon film is carried out, the field shield isolation structure 22 top is straddled, and it is Si 3N4 to band-like on the element formation field 21. The gate electrode 8 which consists of the cap insulator layer 51 and polycrystal silicon film which consist of a film is formed.

[0060] Then, a silicon oxide is formed in the whole surface by CVD, anisotropic etching of the whole surface of this silicon oxide is carried out, the side-attachment-wall protective coat 52 is formed in the side of each gate electrode 8 and the cap insulator layer 51, and the gate electrode structure 53 is formed.

[0061] Next, after forming the BPSG film 54 in about 600nm by ordinary-pressure CVD here [the thickness and here] where the gate electrode structure 53 on the element formation field 21 is embedded after forming a silicon oxide 55 in about 100nm of thickness so that the whole surface may be worn by CVD as shown in drawing 10 (b), and giving a reflow, only about 100-200nm only of thickness carries out polish removal of the surface part of the layer insulation film 54 by the CMP method.

[0062] Next, as shown in drawing 10 (c), whole surface etchback processing is shortly performed to the layer insulation film 54 to which flattening of the front face was carried out to some extent by the CMP method by the dry etching method. Etching gas is made into the mixed gas of CHF3 (60sccm), CF4 (60sccm), and Ar (800sccm), using an parallel monotonous type etching system for example as etching conditions, an etching pressure is set to 1700mTorr(s) and injection power is set to 750W with RF power. Here, if etching of the layer insulation film 54 progresses by etchback processing, the front face of the cap insulator layer 51 of the

gate electrode structure 53 which consists soon on the lower layer field shield isolation structure 22 of the layer insulation film 54 will be exposed. At this time, the etching area of the layer insulation film 54 decreases, and CO emission spectrum intensity in plasma also decreases in connection with it. With this operation gestalt, the variation of this CO emission spectrum intensity is detected, and the time of the cap insulator layer 52 being exposed is specified to the terminal point of etching. In this operation gestalt, repeatability can fully improve the whole surface mostly flattening of the layer insulation film 54 in the minimum thickness by the aforementioned etchback processing following the surface polish by the CMP method.

[0063] although illustration was omitted after an appropriate time -- a memory cell capacitor, a layer insulation film, and connection -- pass processes, such as formation of a hole, and formation of the metal wiring following it, -- an MOS transistor is completed

[0064] As mentioned above, in the 3rd operation gestalt, the front face of the layer insulation film 54 which embeds the gate electrode structure 53 is ground first. Etchback of the front face of the layer insulation film 54 at this time by which flattening was carried out to some extent is carried out. At this time, flattening of the front face of the layer insulation film 54 can fully be carried out, and reduction of a global level difference is made good. However, it is inferior to the polish homogeneity of the layer insulation film 54 and repeatability between the silicon semiconductor substrates 1 within the field of the silicon semiconductor substrate 1, and dispersion in the amount of polishes (**** of the layer insulation film 54) is large. Since etchback is given by using the cap insulator layer 51 as a stopper until the front face of the cap insulator layer 51 located in the lower layer of the layer insulation film 54 is exposed first namely, the end time of etchback is specified certainly. Therefore, the layer insulation film 54 will have a final very high precision, and will be carried out [flattening] by the etchback following polish.

[0065] in addition, the 1- above-mentioned [this invention] -- it is not limited to the 3rd operation ****** For example, instead of forming isolation structure as field shield isolation structure by the field shield isolation method, it forms as a field oxide film by the so-called LOCOS method, or a slot is formed in a silicon semiconductor substrate by the trench separation method, this Mizouchi may be embedded by the insulator layer and trench type isolation structure may be formed.

[Translation done.]

DESCRIPTION OF DRAWINGS

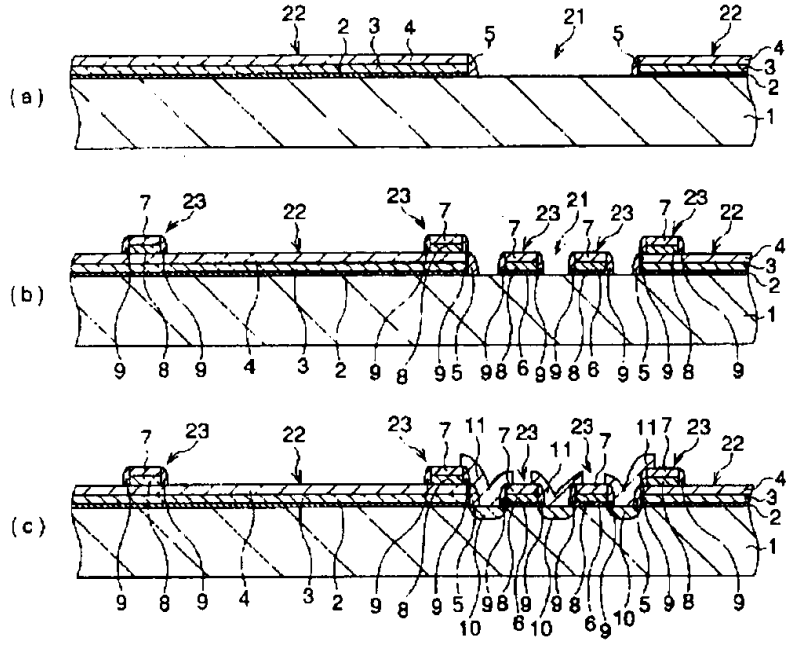
[Brief Description of the Drawings]
[Drawing 1] In the 1st operation gestalt of this invention, it is the outline cross section showing the manufacture method of DRAM in order of a process.
[Drawing 2] It is the outline cross section showing the manufacture method of DRAM in order of a process in the 1st operation gestalt of this invention following on drawing 1.
[Drawing 3] It is the outline cross section showing the manufacture method of DRAM in order of a process in the 1st operation gestalt of this invention following on drawing 2.
[Drawing 4] In the 2nd operation gestalt of this invention, it is the outline cross section showing the manufacture method of DRAM in order of a process.
[Drawing 5] It is the outline cross section showing the manufacture method of DRAM in order of a process in the 2nd operation gestalt of this invention following on drawing 4.
[Drawing 6] It is the outline cross section showing the manufacture method of DRAM in order of a process in the 2nd operation gestalt of this invention following on drawing 5.
[Drawing 7] It is the outline cross section showing the manufacture method of DRAM in order of a process in the 2nd operation gestalt of this invention following on drawing 6.
[Drawing 8] It is the outline cross section showing the manufacture method of DRAM in order of a process in the 2nd operation gestalt of this invention following on drawing 7.
[Drawing 9] It is the outline cross section showing the manufacture method of DRAM in order of a process in the 2nd operation gestalt of this invention following on drawing 8.
[Drawing 10] In the 3rd operation gestalt of this invention, it is the outline cross section showing the manufacture method of an MOS transistor in order of a process.
[Description of Notations]
1 P Type Silicon Semiconductor Substrate
6 Gate Insulator Layer
7, 42, 51 Cap insulator layer
8 Gate Electrode
9 (It Consists of a Silicon Oxide) Side-Attachment-Wall Protective Coat
10 33 Diffusion layer
11 32 Polycrystal silicon pad
12, 13, 14, 25, 34, 38, 44, 54 Layer insulation film
15 Bit Contact -- Hole
16 Polycrystal Silicon Film
17 Tungsten Silicide Film
18 Silicon Nitride
21 Element Formation Field
21a Memory cell field
21b Circumference circuit field
22 Field Shield Isolation Structure
23, 31, 53 Gate electrode structure
24 Bit Wiring
35 Storage Node Electrode
36 Dielectric Film
37 Cell Plate Electrode
43 52 (it consists of a silicon nitride) Side-attachment-wall protective coat

[Translation done.]

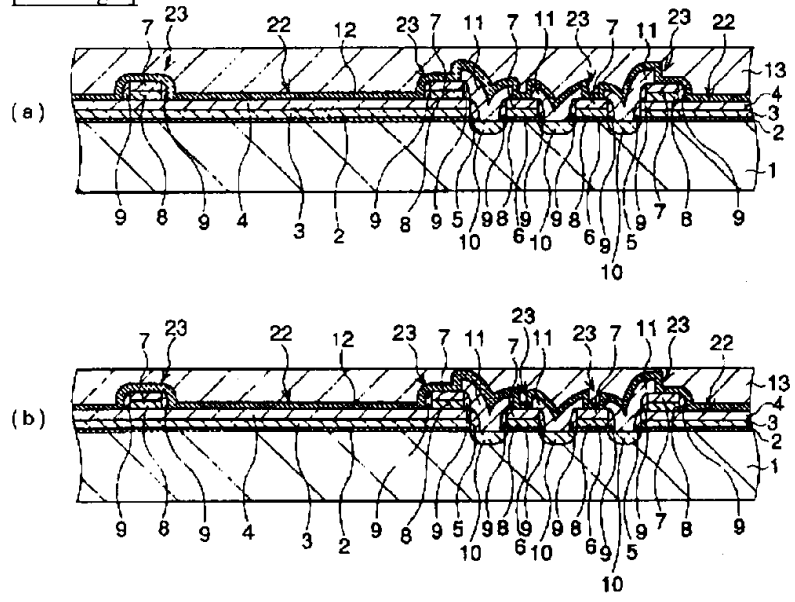
* NOTICES *

DRAWINGS

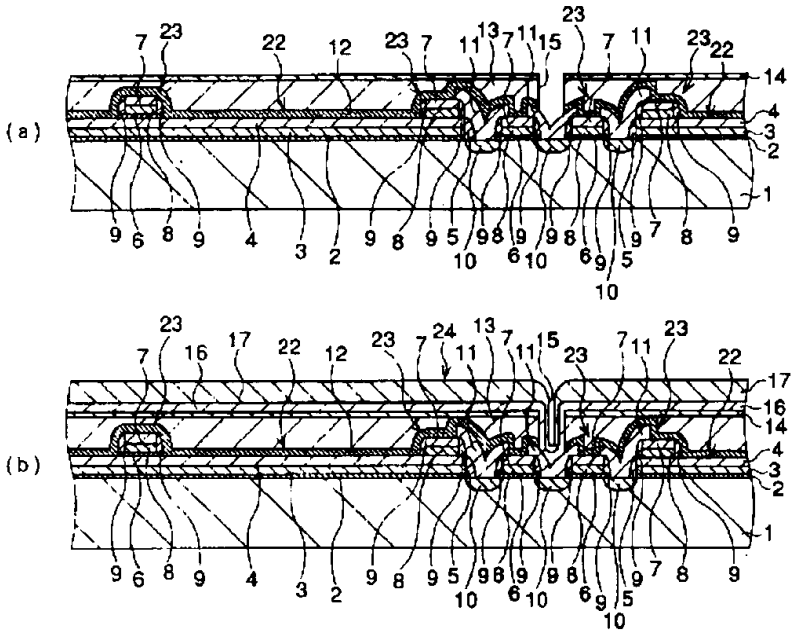
[Drawing 1]



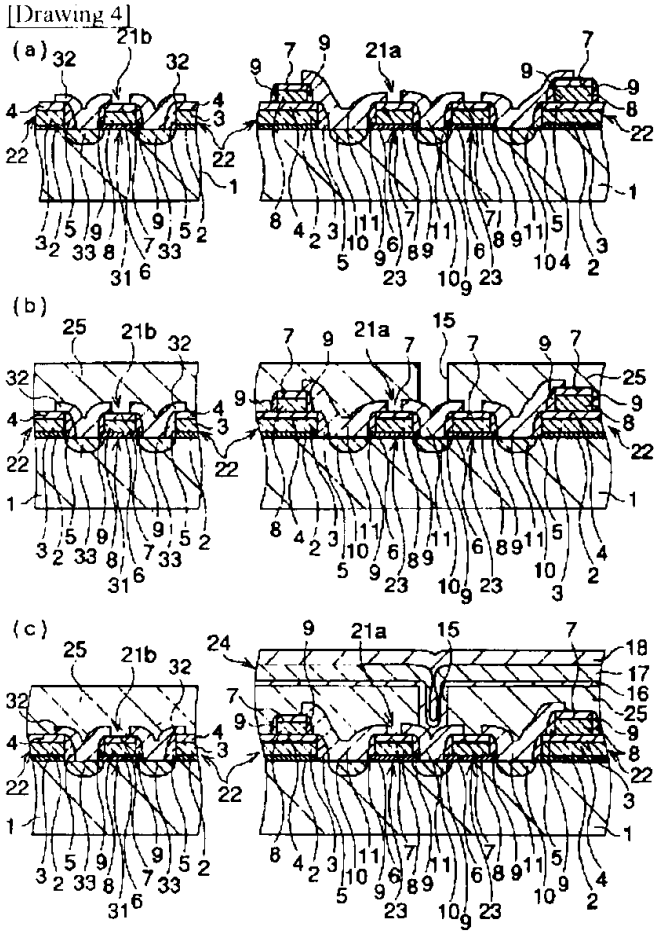
[Drawing 2]



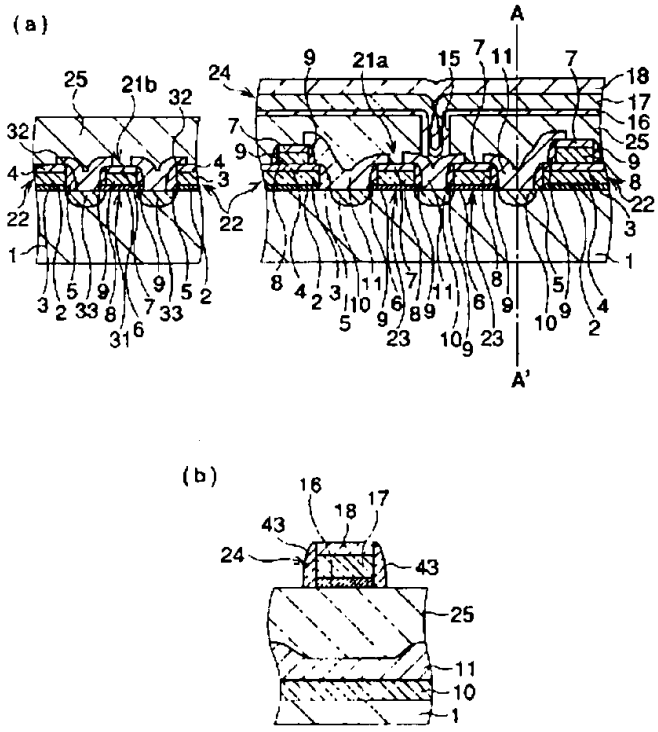
[Drawing 3]



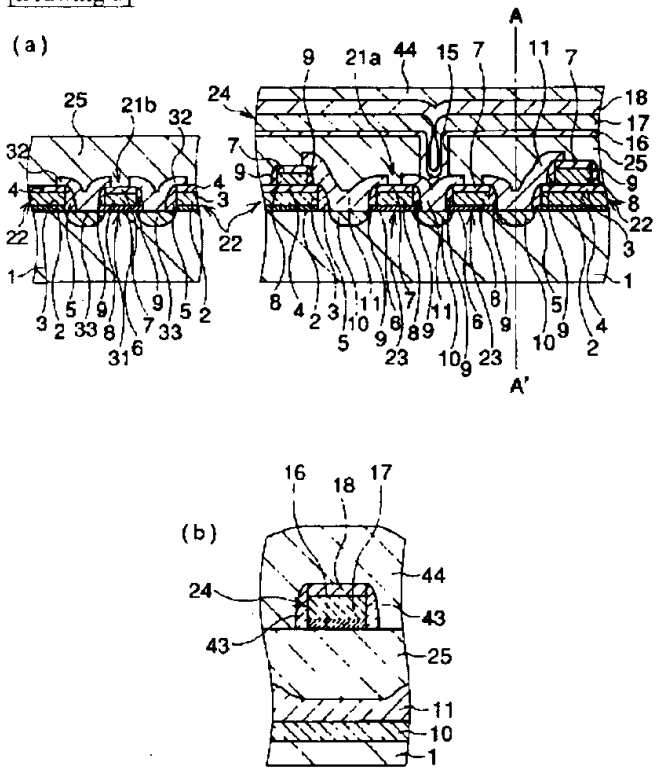
[Drawing 4]



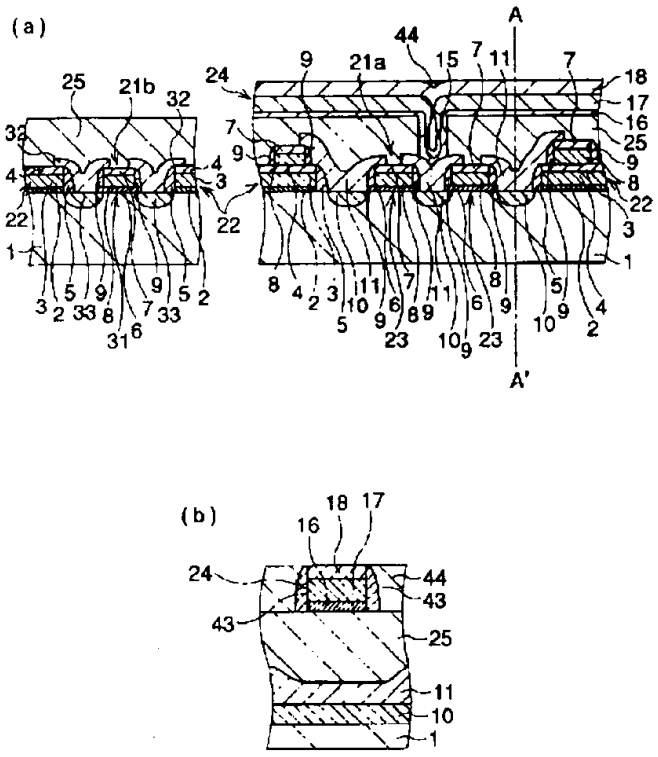
[Drawing 5]



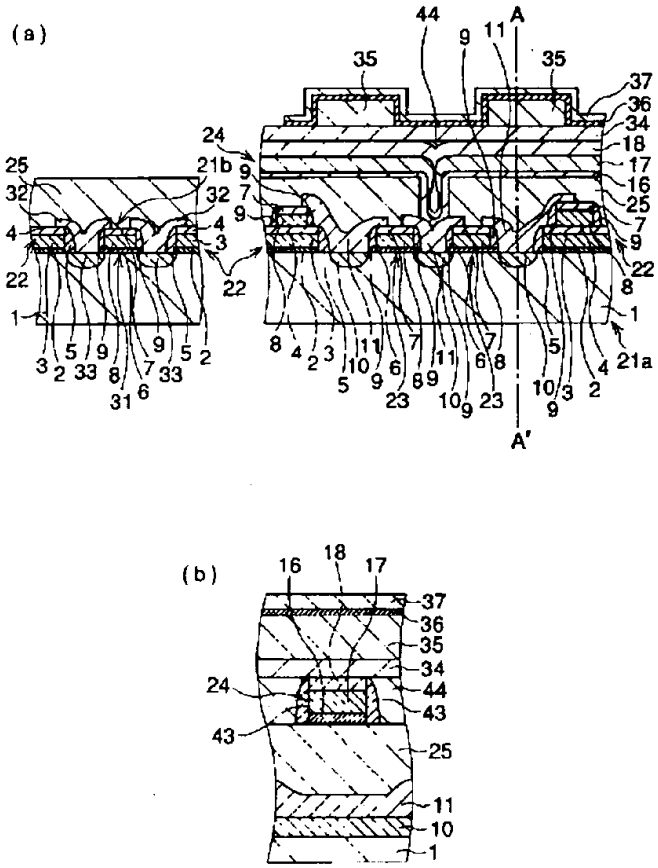
[Drawing 6]



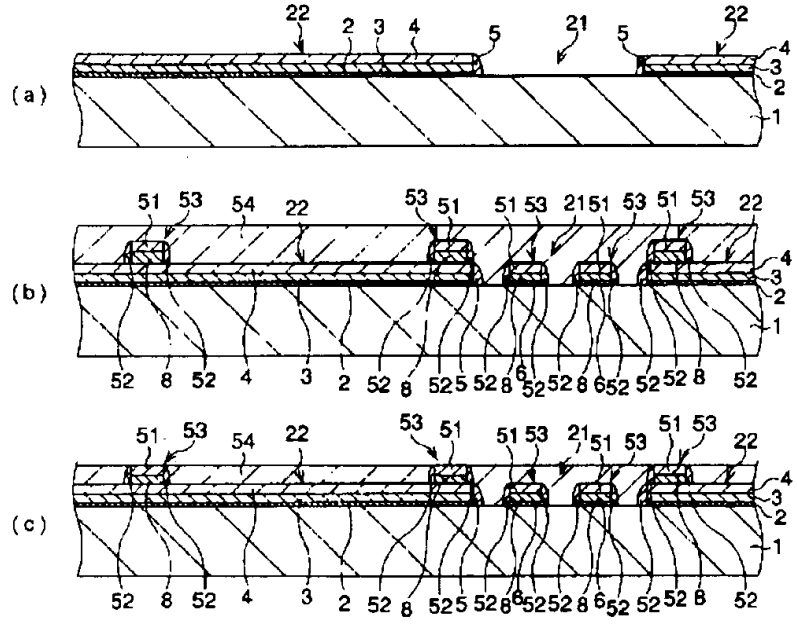
[Drawing 7]



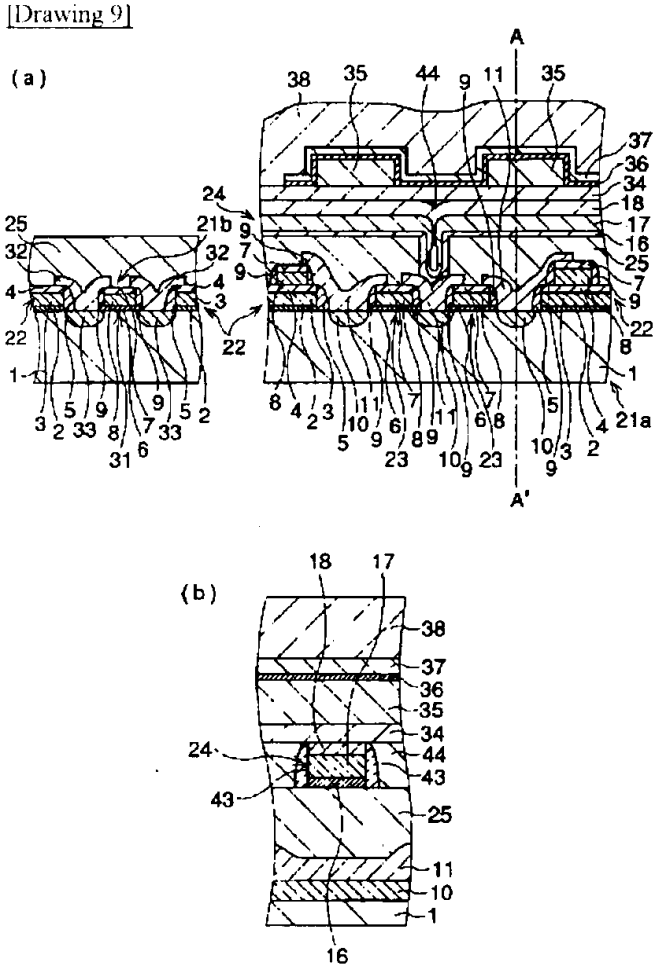
[Drawing 8]



[Drawing 10]



[Drawing 9]



[Translation done.]